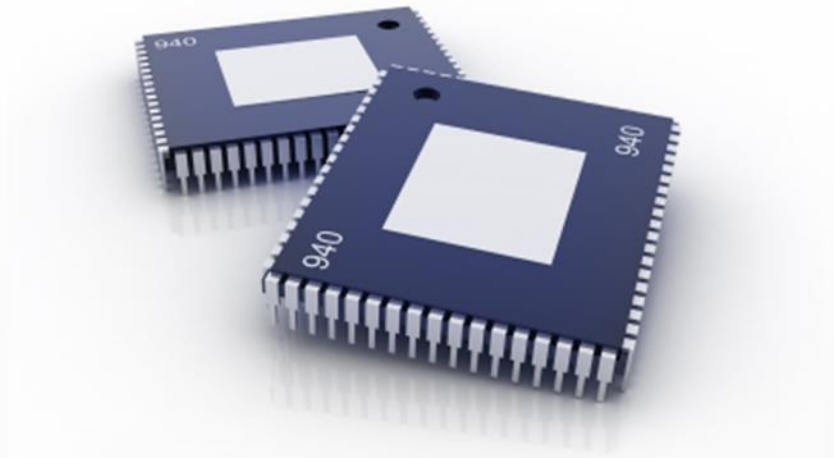

LECTURE 8

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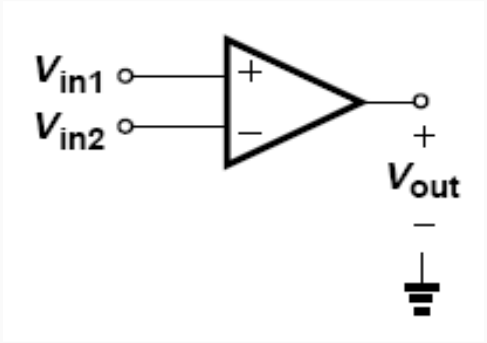
14. Switched-Capacitor Circuits

Basic Building Blocks

Opamps



A operational amplifier

Capacitor

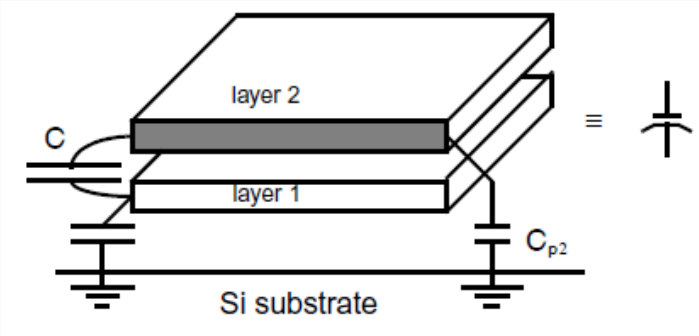


Fig. 14.1 An integrated Circuit capacitor for switched-capacitor circuits

Switches

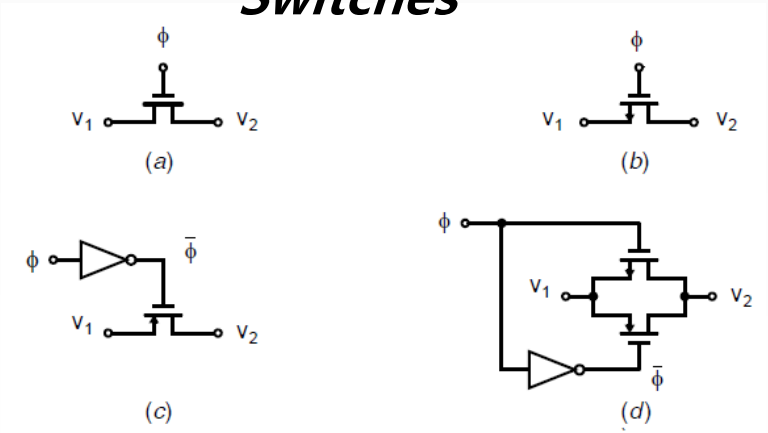


Fig. 14.2 Switch symbol and some transistor circuits

Nonoverlapping Clocks

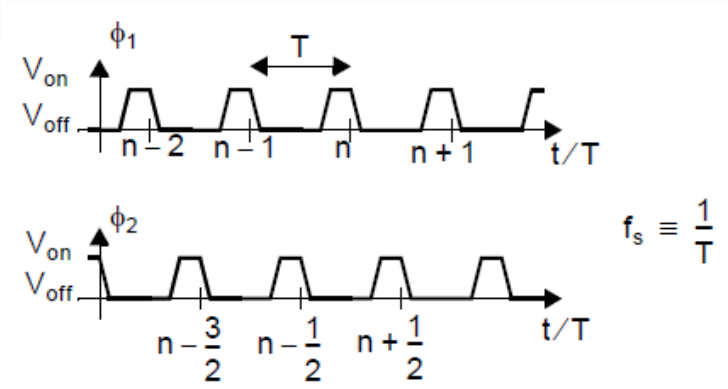


Fig. 14.3 Nonoverlapping clocks

Discrete

Resistor Equivalence of a Switched Capacitor

Switched capacitor resistor

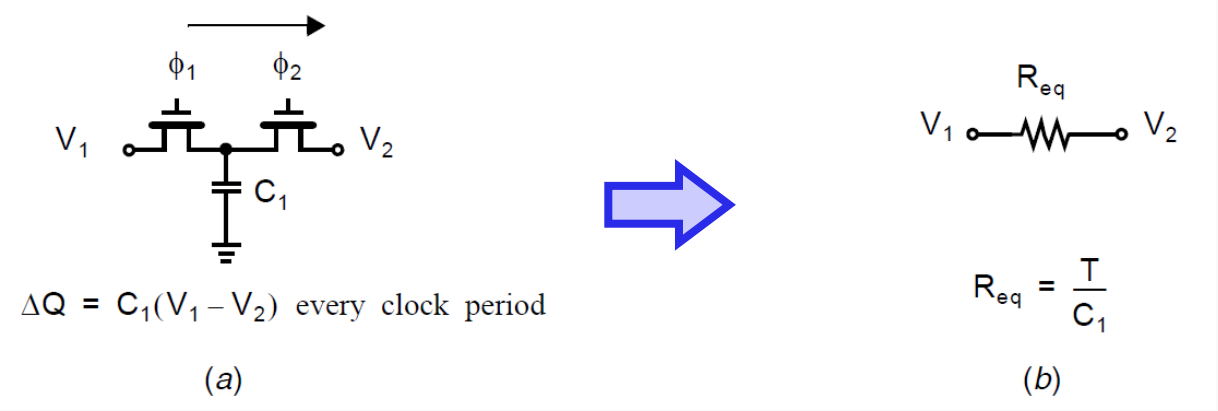


Fig. 14.4 Resistor equivalence of a switched capacitor. (a) Switched-capacitor circuit, and (b) resistor equivalent

$$\Delta Q_1 = C_1\left(V_1 - V_2\right)$$

$$I_{avg} = \frac{C_1\left(V_1 - V_2\right)}{T} \Rightarrow \boxed{R_{eq} = \frac{T}{C_1} = \frac{1}{C_1 f_s}} \quad (14.5)$$

$$I_{eq} = \frac{V_1 - V_2}{R_{eq}}$$

- Tolerant process variation (ex integrator)
- Require non-overlapping clock

Parasitic-Sensitive Integrator

Operation of parasitic-sensitive integrator

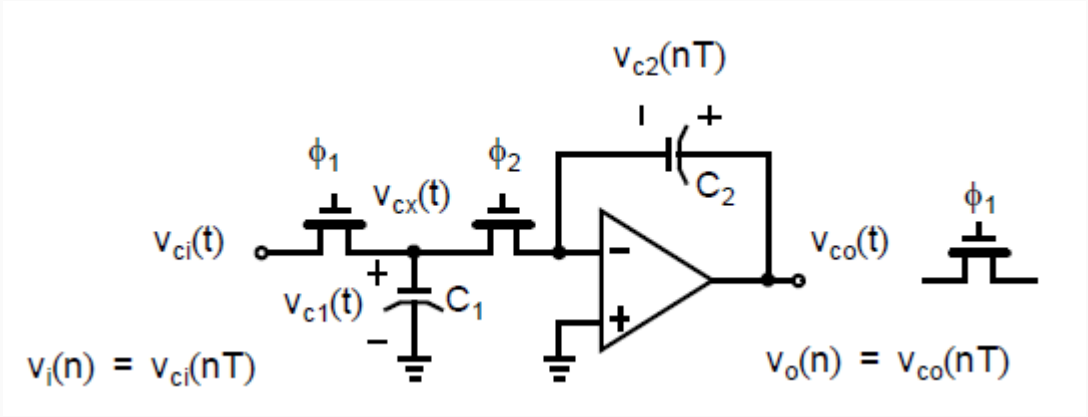
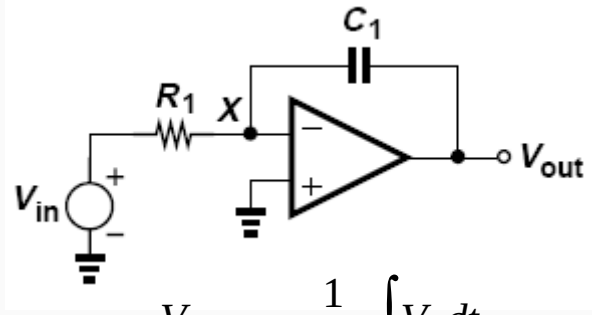
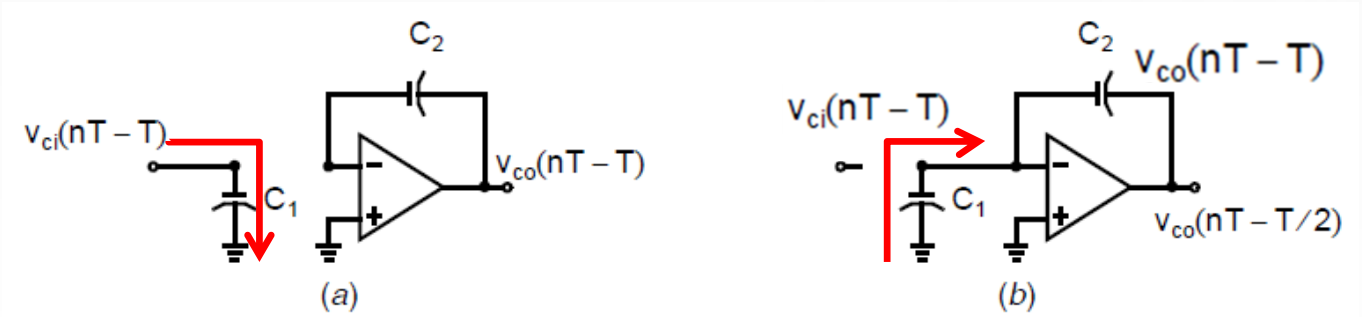


Fig. 14.5 A discrete-time integrator.



$$V_{out} = -\frac{1}{R_1 C_1}\int V_{in}\,dt.$$

Continuous-time integrator.



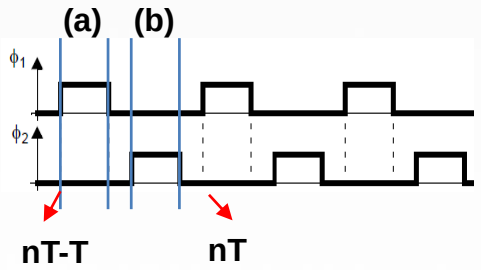


Fig. 14.6 The parasitic-sensitive integrator circuit for the two clock phases.

$$C_2 v_{co}\left(nT - T/2\right) = C_2 v_{co}\left(nT - T\right) - C_1 v_{ci}\left(nT - T\right) \quad (14.12)$$

Parasitic-Sensitive Integrator

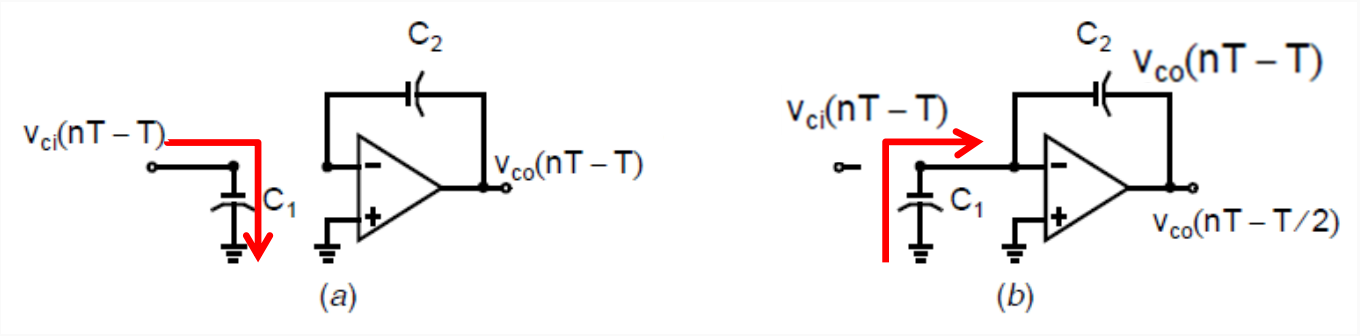


Fig. 14.6 The parasitic-sensitive integrator circuit for the two clock phases.

$$C_2 v_{co}\left(nT - T/2\right) = C_2 v_{co}\left(nT - T\right) - C_1 v_{ci}\left(nT - T\right) \quad (14.12)$$

$$C_2 v_{co}\left(nT\right) = C_2 v_{co}\left(nT - T/2\right) \quad (14.13)$$

$$C_2 v_{co}\left(nT\right) = C_2 v_{co}\left(nT - T\right) - C_1 v_{ci}\left(nT - T\right) \quad (14.14)$$

Assume $T = 1$,

$$v_o\left(n\right) = v_o\left(n-1\right) - \frac{C_1}{C_2} v_i\left(n-1\right) \quad (14.15)$$

$$V_o\left(z\right) = z^{-1} V_o\left(z\right) - \frac{C_1}{C_2} z^{-1} V_i\left(z\right) \quad (14.16)$$

z-transform($v_o\left(n-1\right) \Rightarrow z^{-1} \cdot V_o\left(z\right)$)

$$H\left(z\right) \equiv \frac{V_o\left(z\right)}{V_i\left(z\right)} = -\left(\frac{C_1}{C_2}\right)\frac{1}{z-1} \quad (14.18)$$

Discrete-time integrator

Parasitic-Sensitive Integrator

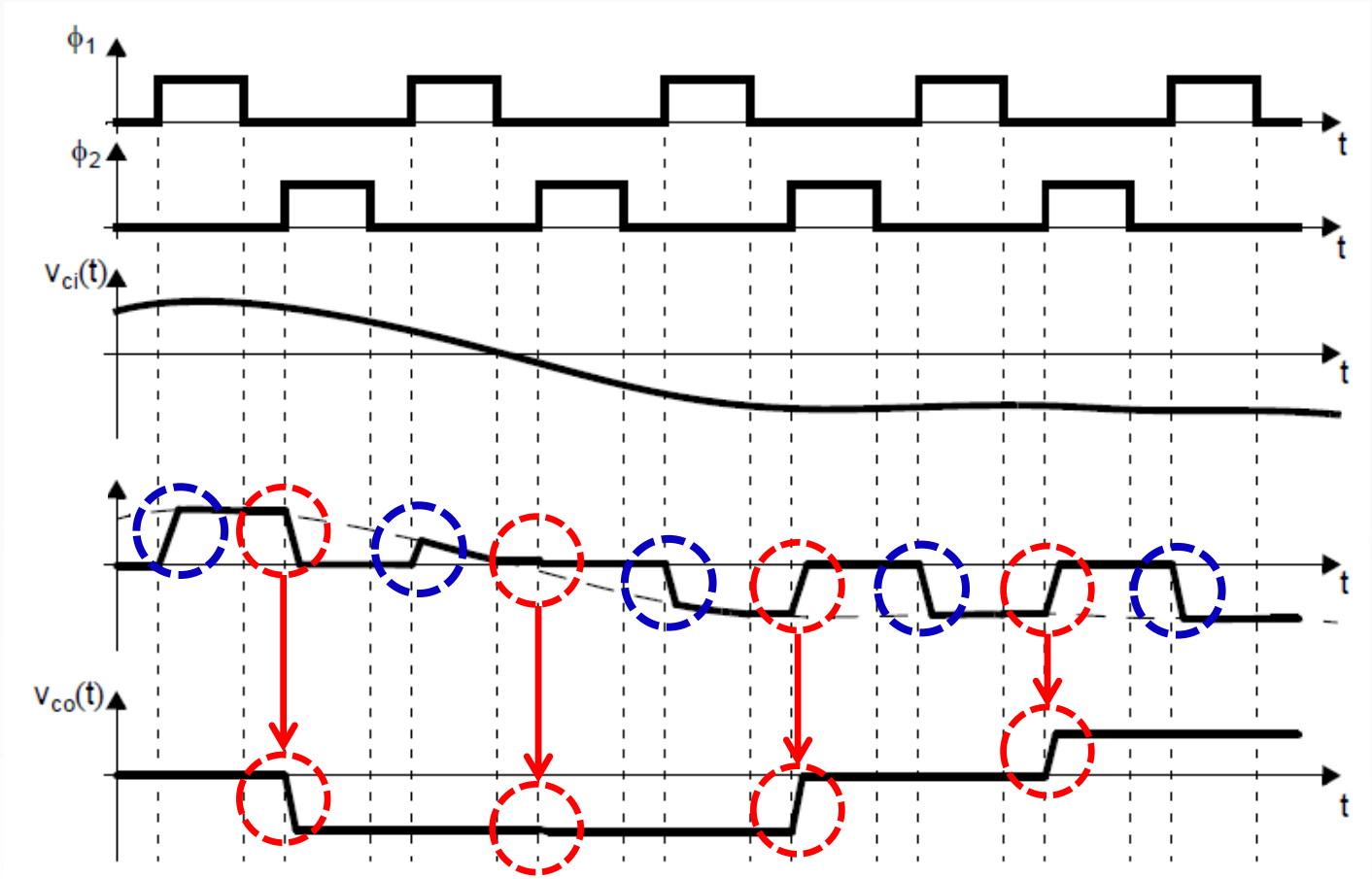


Fig. 14.7 Typical voltage waveforms for the discrete-time integrator shown in Fig. 14.5.

: Sampling : Transfer

Parasitic-sensitive Integrator

Problem of previous integrator

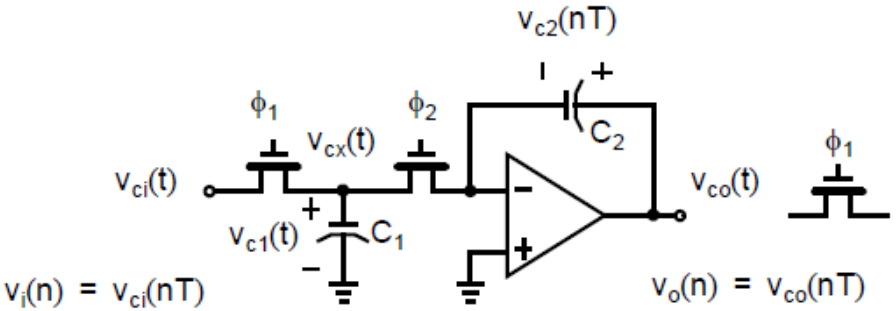


Fig. 14.5 A discrete-time integrator.

Affect only the speed

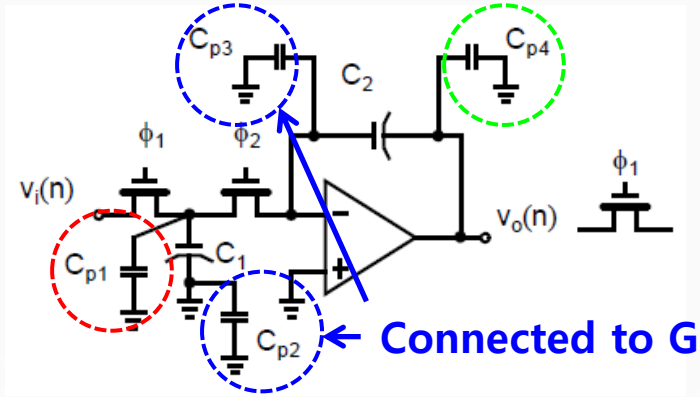


Fig. 14.8 A discrete-time integrator with parasitic capacitance shown.

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right)\frac{1}{z-1}$$

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1 + C_{p1}}{C_2}\right)\frac{1}{z-1}$$

Parasitic sensitive!

Parasitic-insensitive Integrator

Parasitic-insensitive integrator

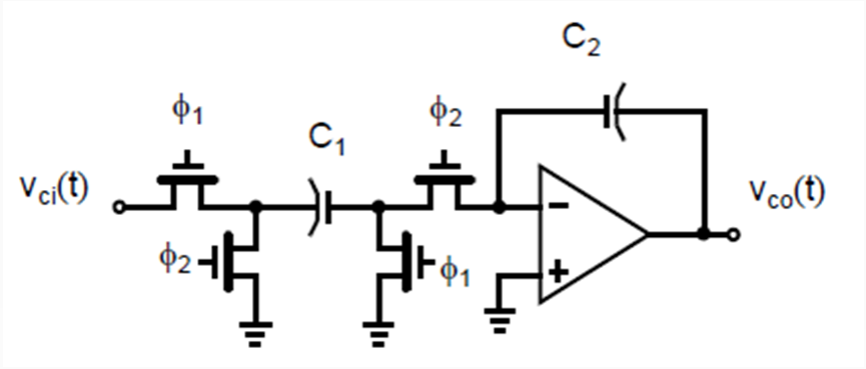


Fig. 14.9 A noninverting delaying discrete-time integrator that is not sensitive to parasitic capacitances.

Same as before

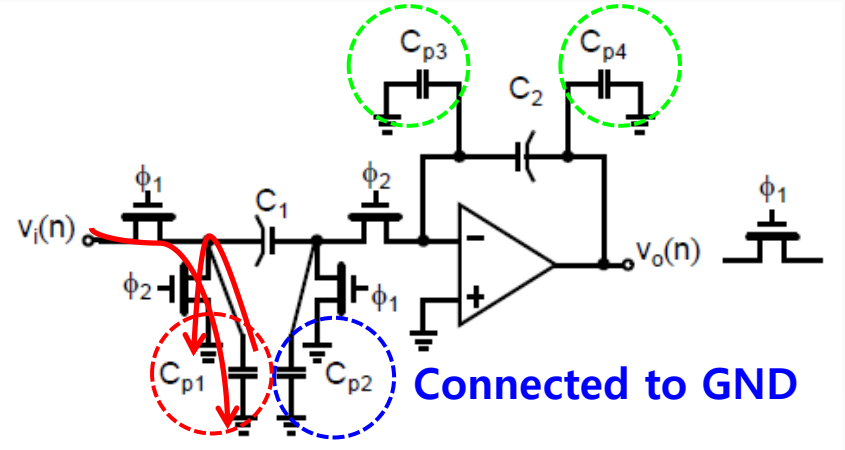


Fig. 14.11 A parasitic-insensitive delayed integrator with parasitic capacitance shown.

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = \left(\frac{C_1}{C_2}\right)\frac{1}{z-1}$$

Parasitic insensitive

More switches(charge injection ↑)