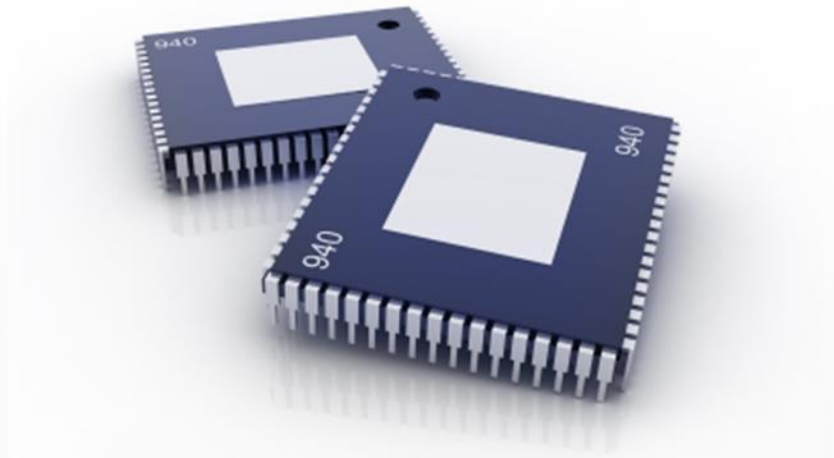



# LECTURE 10

**Soo-Won Kim**

**swkim@korea.ac.kr**

# 11. Sample-and Hold and Translinear Circuit

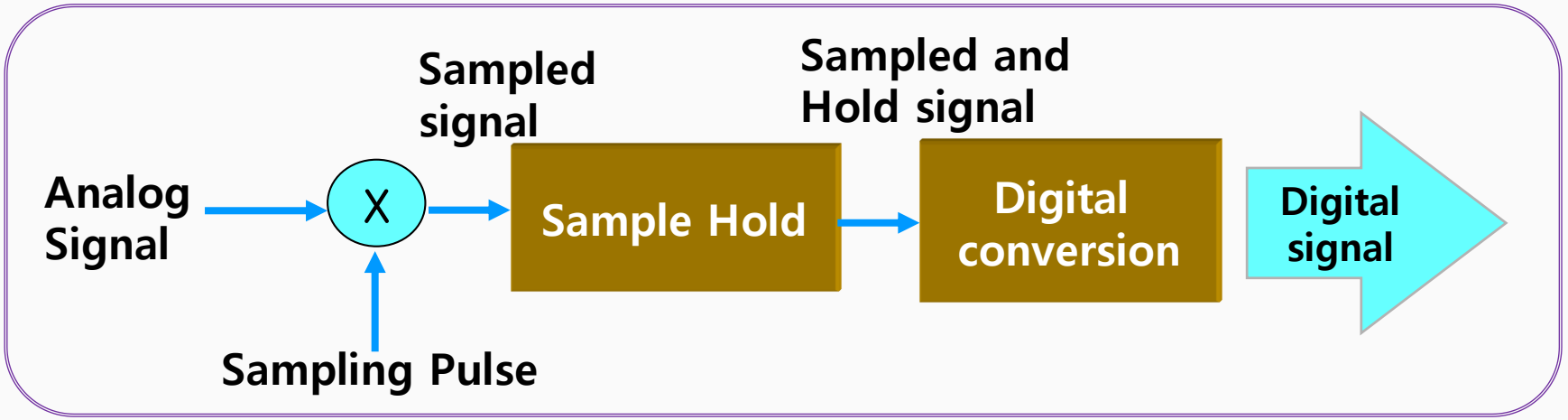
**11.1 Performance of sample-and-hold circuits**

**11.2 MOS sample-and-hold basic**

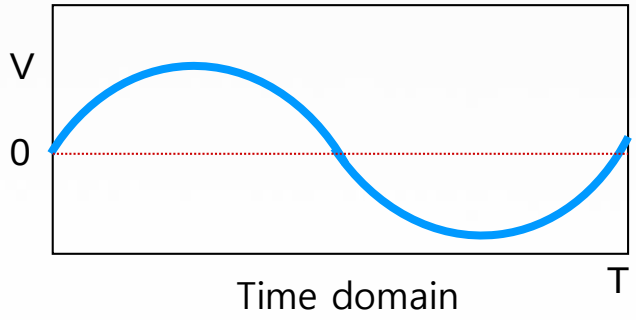
**11.3 Examples of CMOS S/H circuits**

# Sample-and-hold circuit

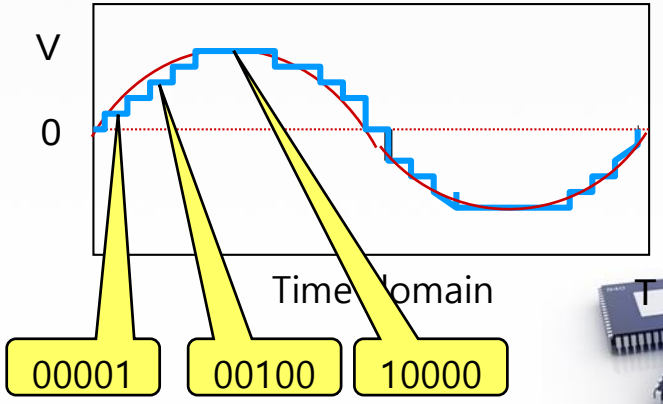
## Analog to digital converter



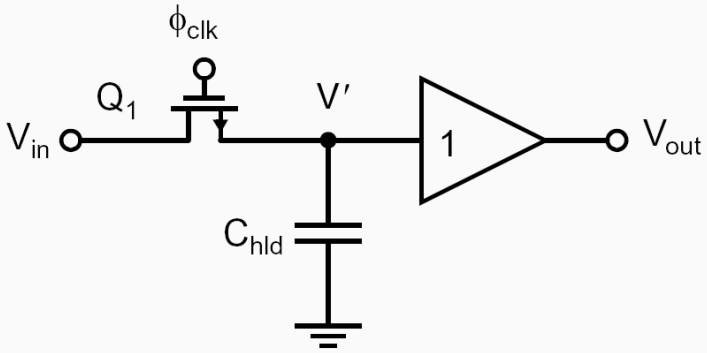

(1) Analog signal




(2) Sampled and Hold signal




# MOS sample-and-hold basics




❖ **Operation**

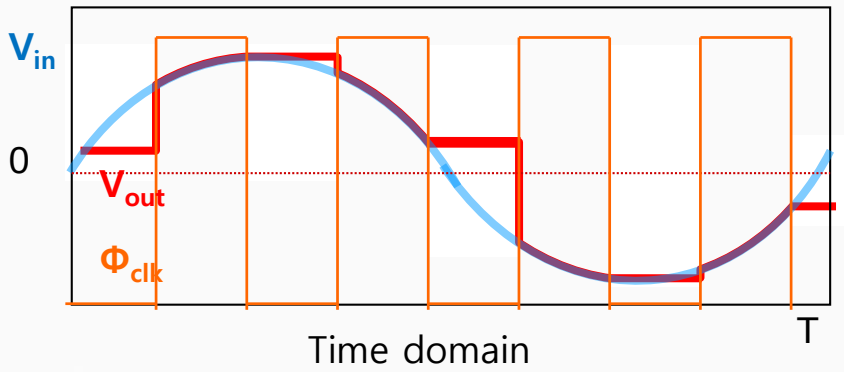



**Fig. 11.3 An open-loop track and hold realized using MOS technology**

- When $\Phi_{clk}$ is closed ⇨ $V_{out}$ samples $V_{in}$

- When $\Phi_{clk}$ is opened ⇨ Vout holds(keep value)

❖ **Problem**

1) **Charge injection(ΔV')** ⇨ $$\Delta V' = \frac{\Delta Q_{C-hld}}{C_{hld}} = -\frac{C_{ox}WL\left(V_{DD} - V_{tn} - V_{in}\right)}{2C_{hld}} \quad (11.3)$$

2) **Low input impedance(lower than Amp)**

# Example 11.1

**Find the hold step for $V_{in}$ equal to 1 V, 0.5V and 0.05V.**

**Estimate the average dc offset**

$$C_{hld}=1pF,\ C_{ox}=8.5\,fF/(\mu m)^2,\ V_{tn}=0.45V,\ (W/L)_1=(5/0.4),\ V_{DD}=2V$$

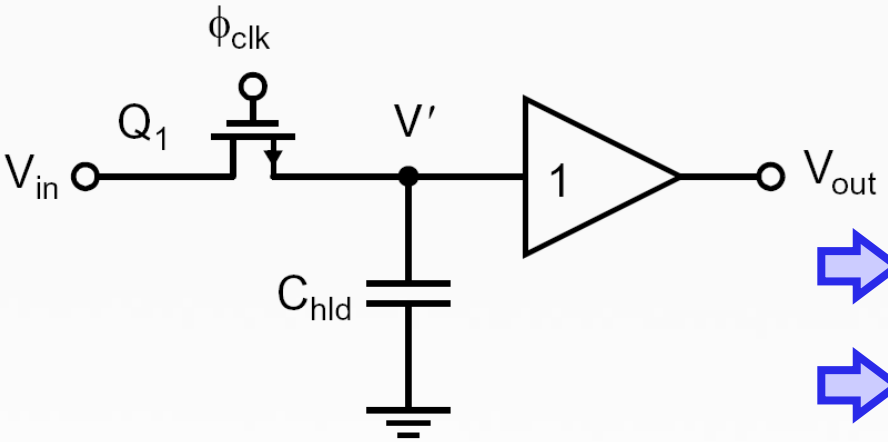



Fig. 11.3 An open-loop track and hold realized using MOS technology

**Using (11.3)**

$$\Delta V' = \frac{\Delta Q_{C-hld}}{C_{hld}} = -\frac{C_{ox}WL\left(V_{DD}-V_{tn}-V_{in}\right)}{2C_{hld}} \qquad (11.3)$$

$$\Delta V'(1V) = -\frac{8.5f\cdot 5\cdot 0.4(2-0.45-1)}{2p} = -4.7mV$$

$$\Delta V'(0.5V) = -\frac{8.5f\cdot 5\cdot 0.4(2-0.45-0.5)}{2p} = -8.9mV$$

$$\Delta V'(0.05V) = -\frac{8.5f\cdot 5\cdot 0.4(2-0.45-0.05)}{2p} = -12.75mV$$

**Average dc offset** $V_{offset-avg} = \dfrac{\Delta V'(1V)+\Delta V'(0.5V)+\Delta V'(0.05V)}{3} = -8.78mV$

**$V_{in}$ ↓ → ΔV′(charge injection voltage) ↑**

# Reduced charge injection

❖ **Problem**

## 1) Charge injection

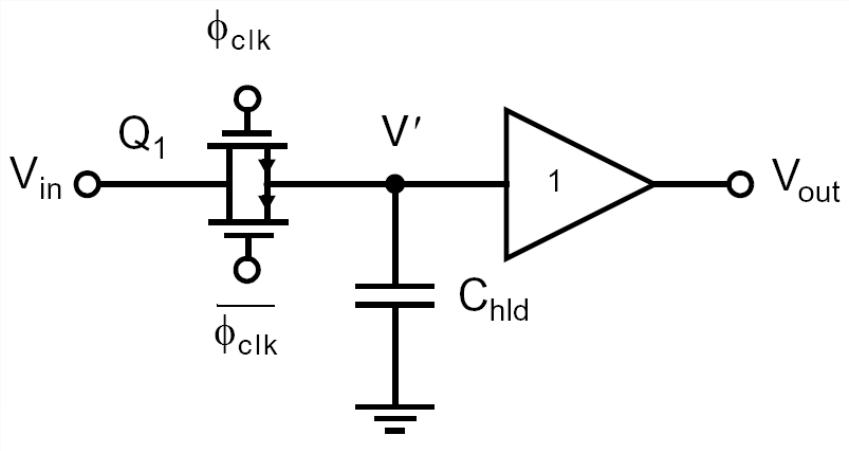



Fig. 11.4 An open-loop track and hold realized using a CMOS transmission gate

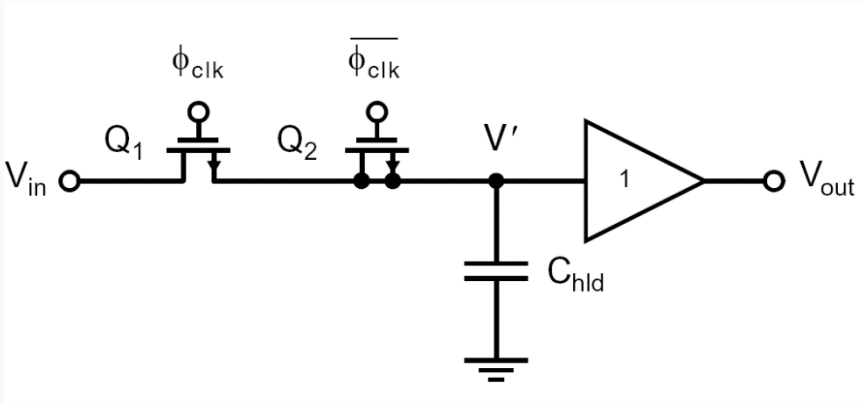



Fig. 11.3 An open-loop track and hold realized using an n-channel switch a long with a dummy switch

**By transmission gate**

☺ **Reduced the charge injection**

☹ **Difficult to make up p and n transistors match**

**Difficult to make clocks fast enough**

**By Dummy switch**

☺ **Reduced the charge injection**

☹ **Difficult to make clocks fast enough**

# High input impedance

❖ **Problem**

**2) Low input impedance**

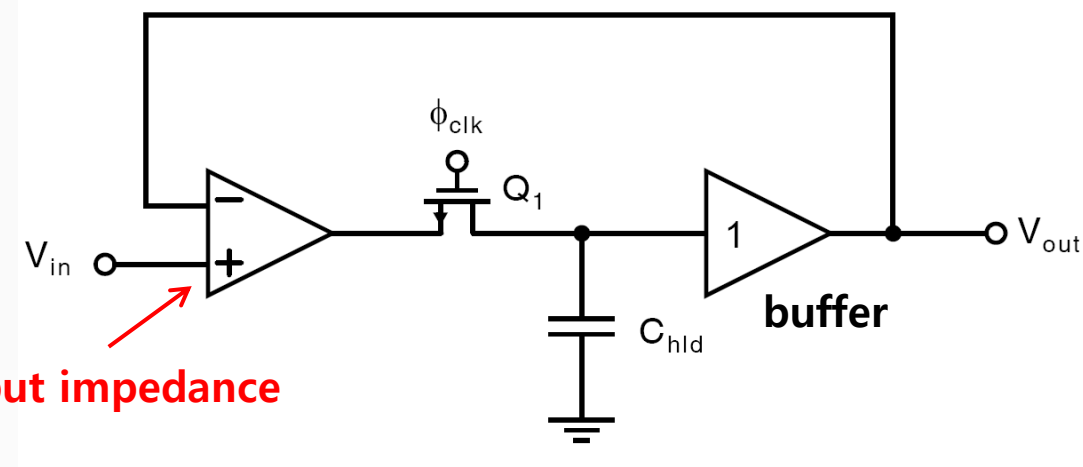



**Fig. 11.7 Including an opamp in a feedback loop of a sample-and-hold to increase the input impedance**

## Advantages

1) High input impedance
2) Dc offset of buffer divided by loop gain

# High input impedance

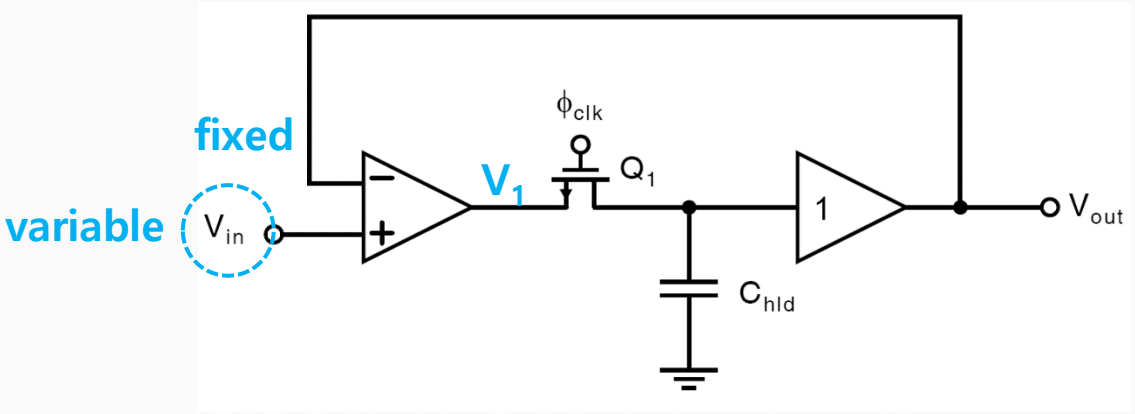
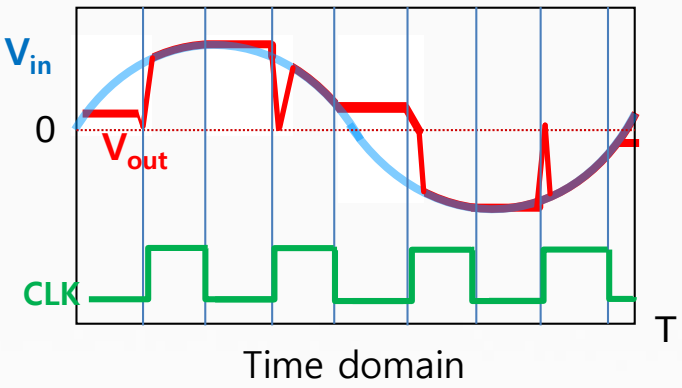



Fig. 11.7 Including an opamp in a feedback loop of a sample-and-hold to increase the input impedance

❖ **Operation**




## Disadvantages

1) In hold mode, $V_1$ saturate at VDD or GND
2) Speed of operation can be degraded
3) Power consumption ↑

# Reduced slew rate requirement

❖ **Problem**

1) **In hold mode, $V_1$ saturate at VDD or GND**

❖ **Operation**

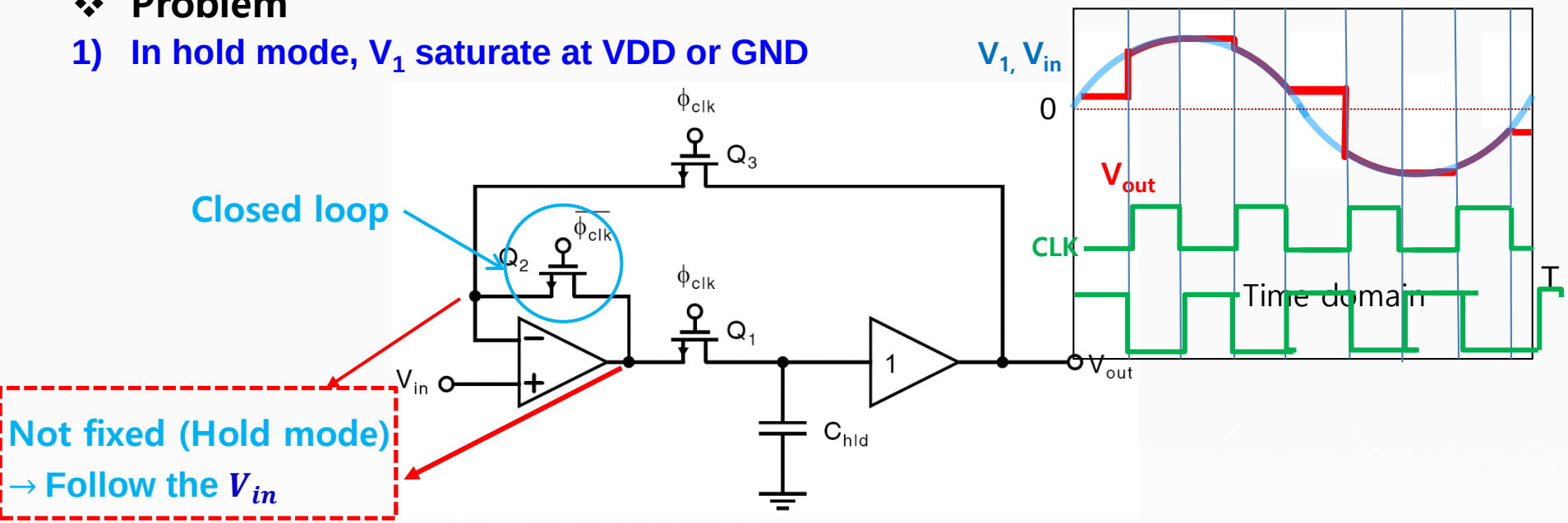



**Fig. 11.8 Adding an additional switch to the S/H of Fig. 11.7 to minimize slewing time**

## Sample-and-hold with an additional switch

- Minimize the slewing time
- **Charge injection, buffer offset**

# Input signal independence

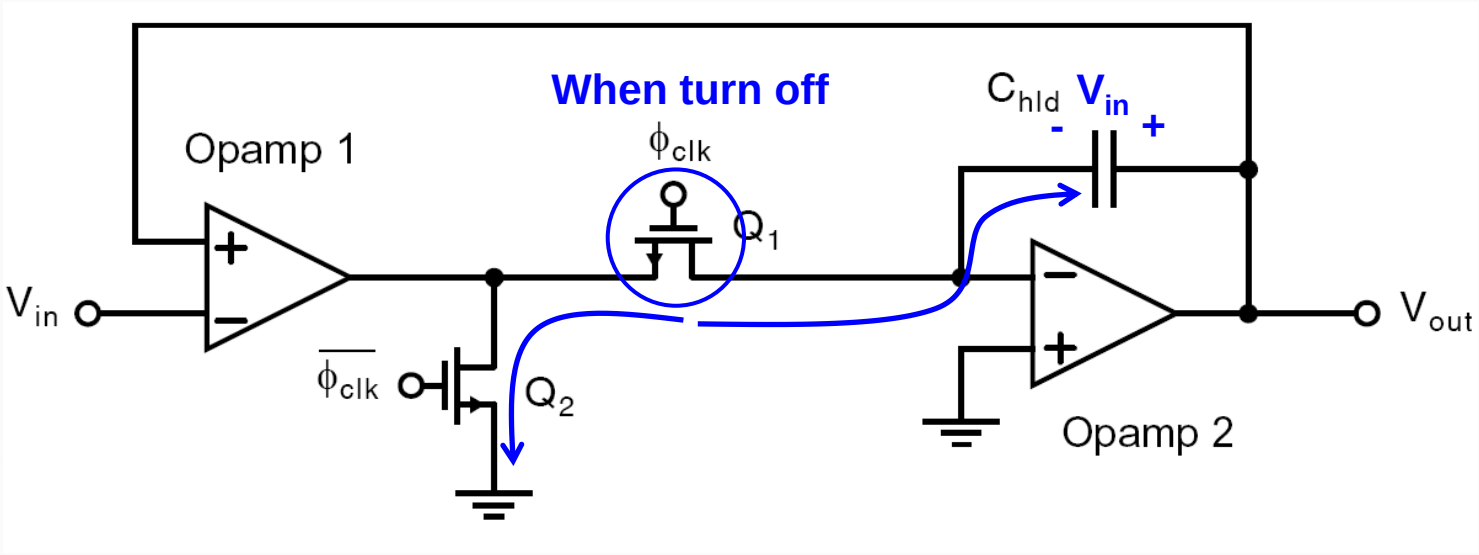



**Fig. 11.9 An improved configuration for an S/H as compared to that of Fig. 11.8.**

## Improved configuration

- When hold mode, Input signal is independent
  $C_{hld}$ → charge the $V_{in}$

- **Charge injection**

# Example 11.2

**Find $C_{hld}$ such that the maximum error in the held voltage is limited to less than 1mV for S/H circuit (Fig. 11.7, 11.9).**

$$C_{ox}=1.92\,fF/(\mu m)^2, V_{tn}=0.8V, (W/L)_1=(5/0.8)\,\mu m/\mu m, V_{DD}=2.5V, V_{in}=\pm 1V$$

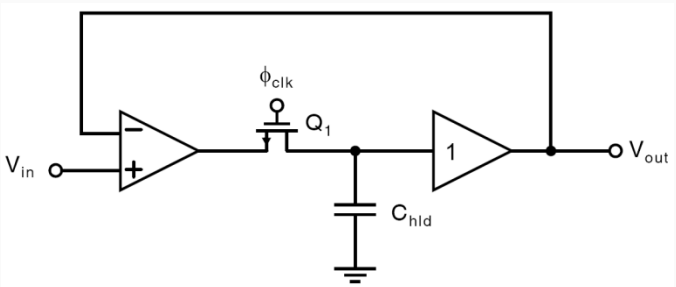



Fig. 11.7 Including an opamp in a feedback loop of a sample-and-hold to increase the input impedance

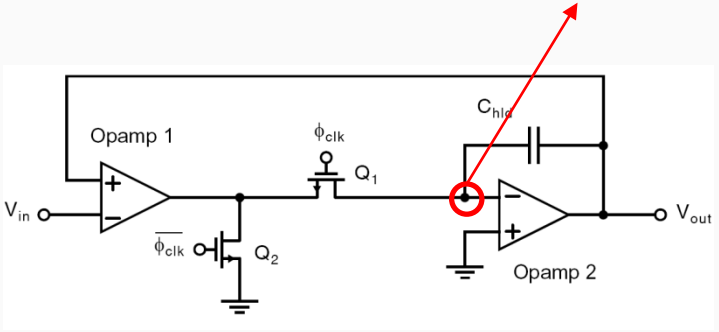



Fig. 11.9 An improved configuration for an S/H as compared to that of Fig. 11.8.

$$\Delta V' = \frac{\Delta Q_{C-hld}}{C_{hld}} = -\frac{C_{ox}WL\left(V_{DD}-V_{tn}-V_{in}\right)}{2C_{hld}} \quad (11.3)$$

$$\rightarrow \frac{1.92f\cdot 5\cdot 0.8\left(2.5-0.8-(-1)\right)}{2C_{hld}} \le 1mV$$

$$\rightarrow C_{hld} \ge 10.37\,pF$$

$$\Delta V' = \frac{\Delta Q_{C-hld}}{C_{hld}} = -\frac{C_{ox}WL\left(V_{DD}-V_{tn}\right)}{2C_{hld}}$$

$$\rightarrow \frac{1.92f\cdot 5\cdot 0.8\left(2.5-0.8\right)}{2C_{hld}} \le 1mV$$

$$\rightarrow C_{hld} \ge 6.525\,pF$$

**$C_{hld}$ is reduced by 62%**

# Reduced offset

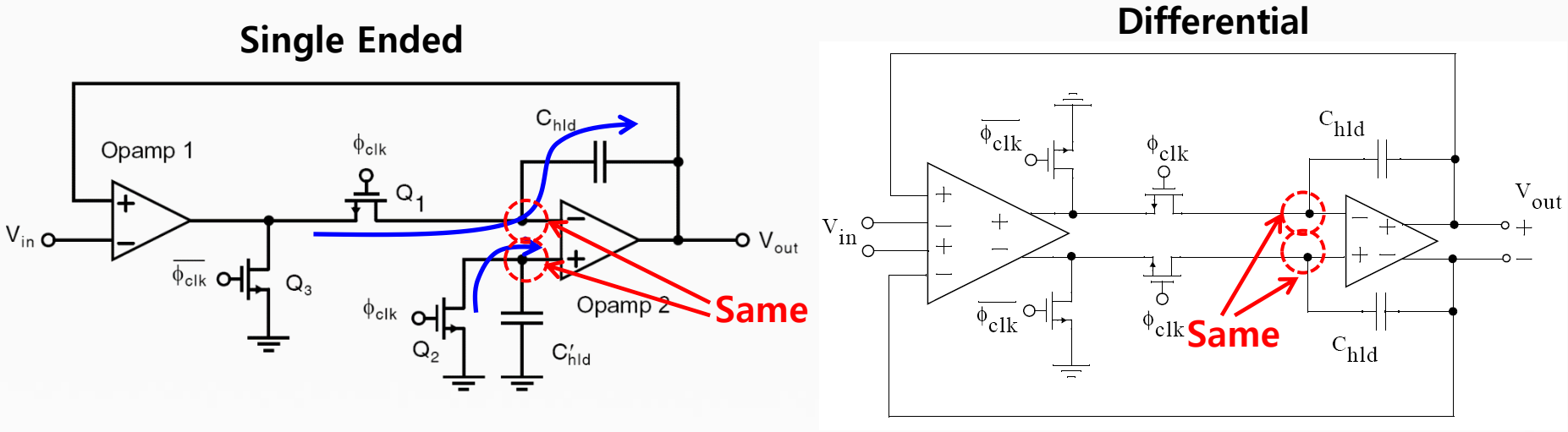



**Fig. 11.10 An S/H similar to that of Fig. 11.9, but with clock-feedthrough cancellation circuitry added**

**Reduced offset circuit**

Charge injected by Q1 matched by Q2 into $C_{hld}$ or $C'_{hld}$