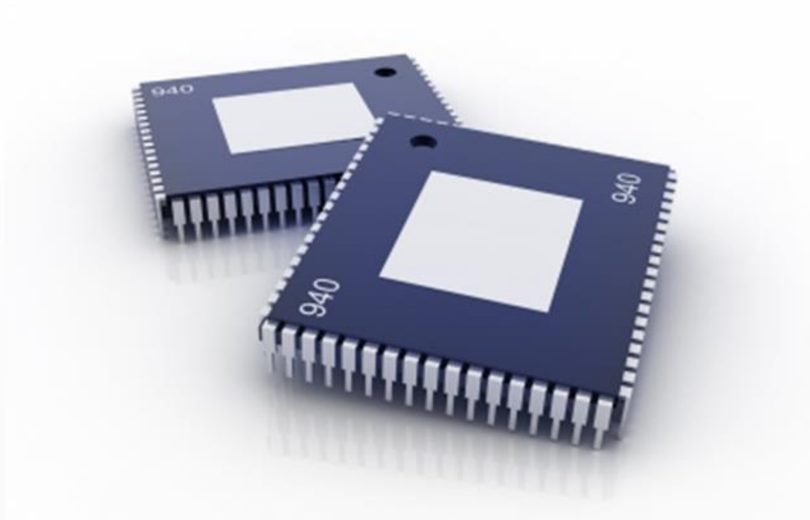

LECTURE 9

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10. Comparators

10.1 Comparator Specifications

10.2 Using an Opamp for a Comparator

10.3 Charge-Injection Errors

ADC block diagram

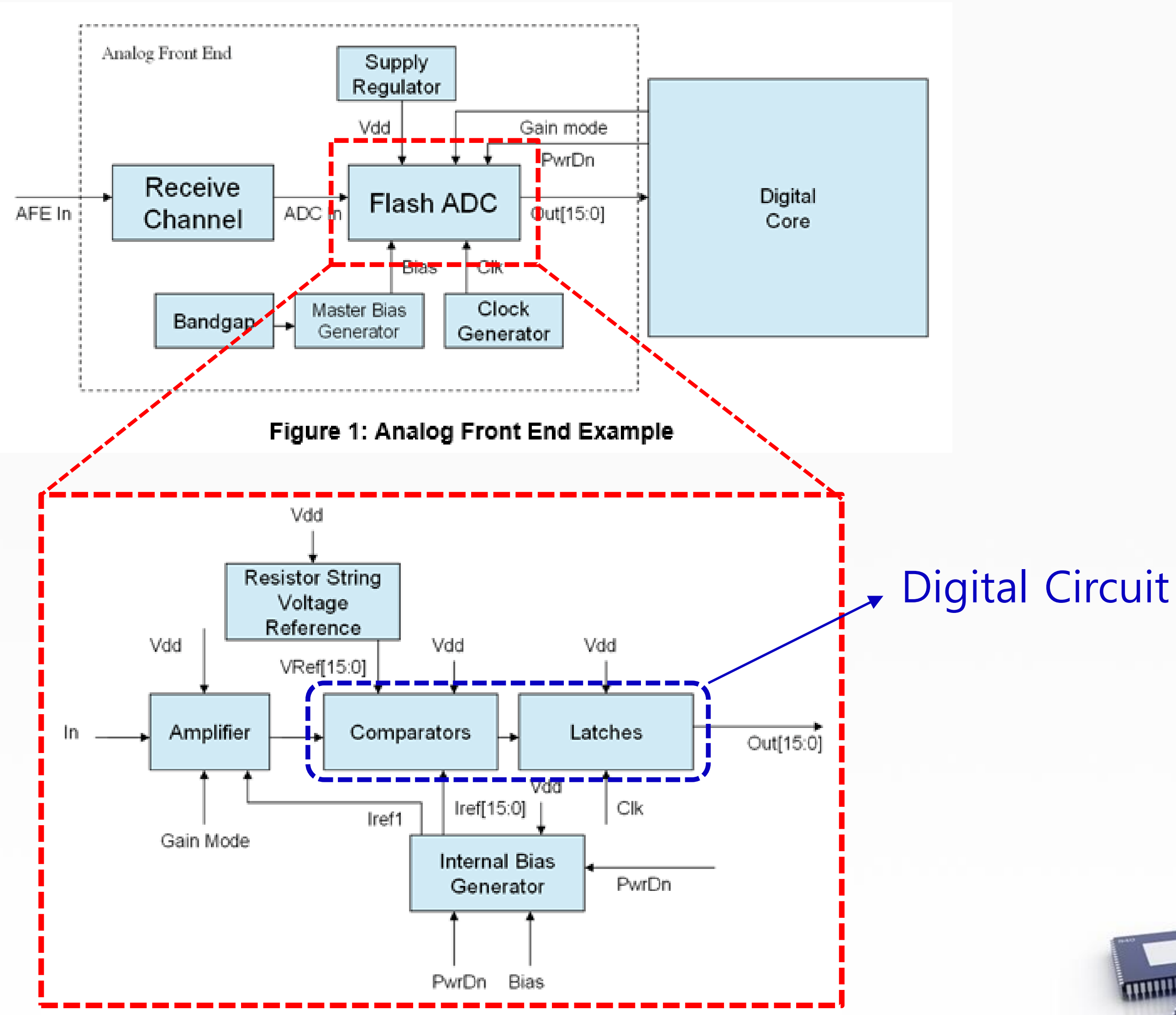


Figure 1: Analog Front End Example

Figure 3: ADC Block Diagram

Open-loop opamp for a comparator

Simplistic approach

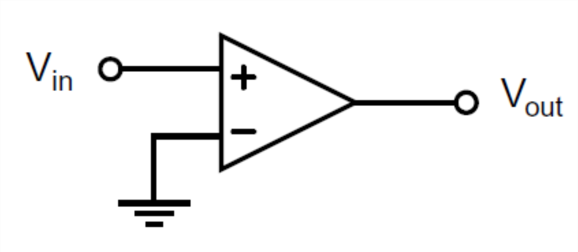


Fig. 10.2 A simplistic approach of using an open-loop opamp for a comparator

Operation

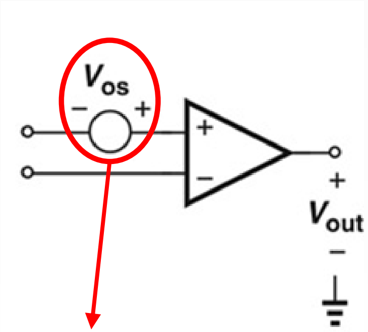
$V_{in} > 0 \rightarrow V_{out} = V_{DD}$

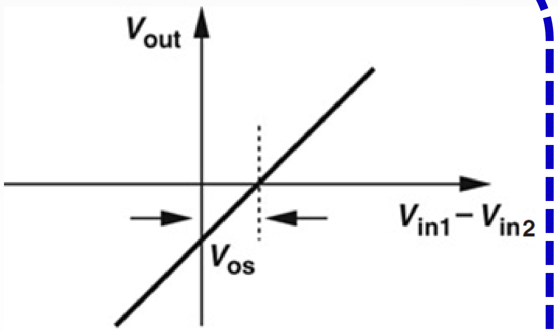
$V_{in} < 0 \rightarrow V_{out} = 0$

Compare the input with ground!!

- Simple to implement
- Limited input-offset voltage

What is offset?





Cause of offset
: Device Mismatches

Recall *Analog CMOS I.C (Razavi)* ch.13.2

Input-Offset Voltage Errors

< Limited input-offset voltage >

Switched-capacitor comparators

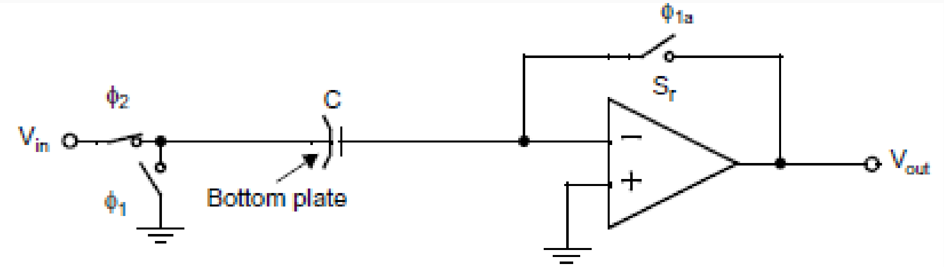


Fig. 10.3

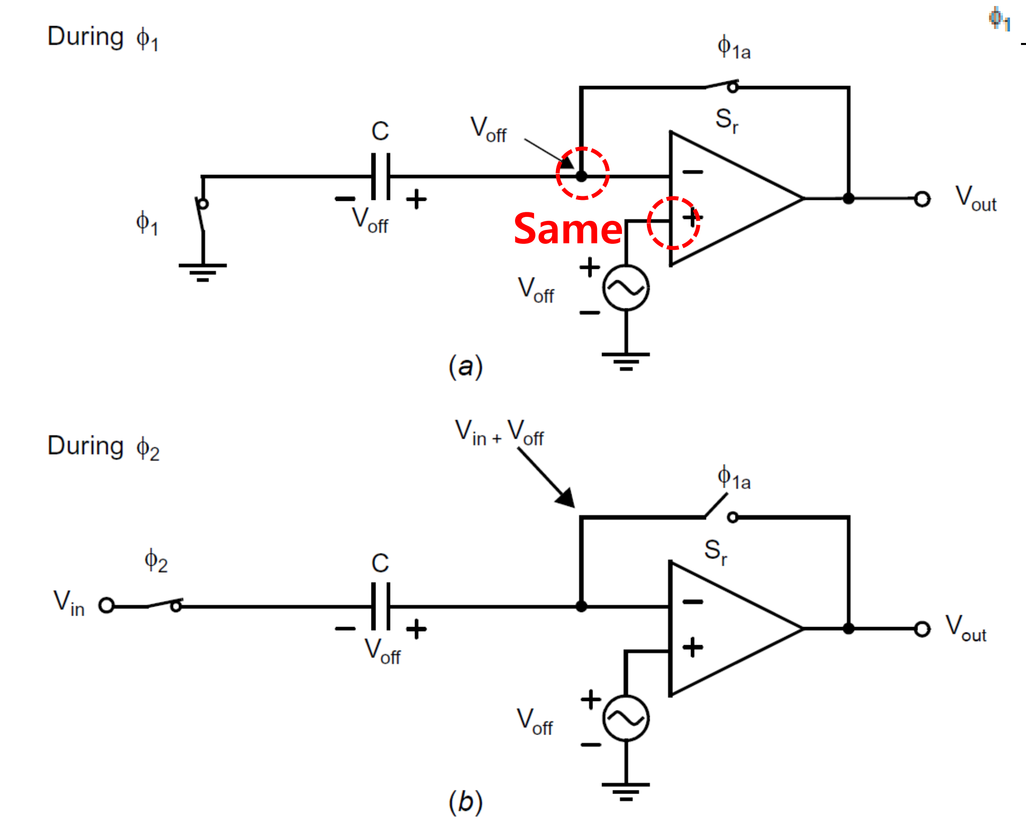


Fig. 10.6 The circuit configuration (a) during the reset phase, (b) during the comparison phase

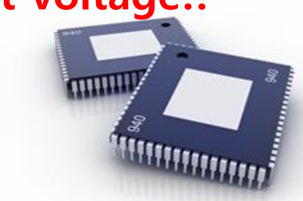
- When ϕ_1 is closed and ϕ_{1a} is closed

$$V_{in+} = V_{in-} = V_{off}$$

- When ϕ_2 is closed and ϕ_{1a} is opened

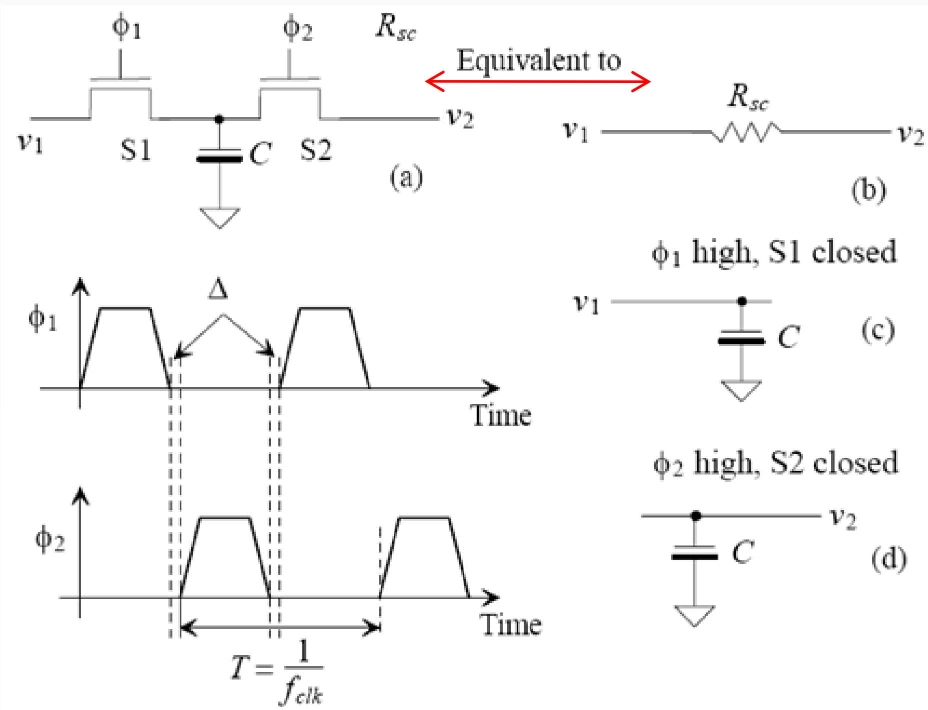
$$V_{in+} = V_{off}$$
$$V_{in-} = V_{off} + V_{in}$$

Eliminate input-offset voltage!!



Switched-capacitor?

Switched-capacitor comparators



Switched-capacitor resistor (a) and associated waveforms and (b,c,d) the equivalent circuits

- When ϕ_1 is high and ϕ_2 is low

$$q_1 = Cv_1$$

- When ϕ_2 is high and ϕ_1 is low

$$q_2 = Cv_2$$

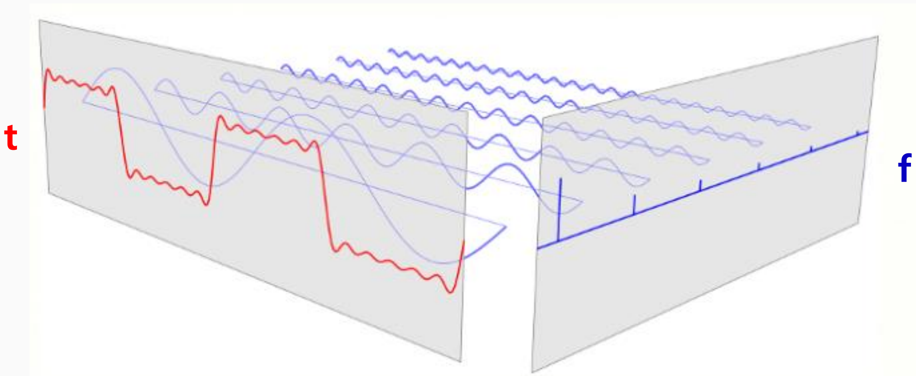
- If $v_1 \neq v_2$, charge equal to difference

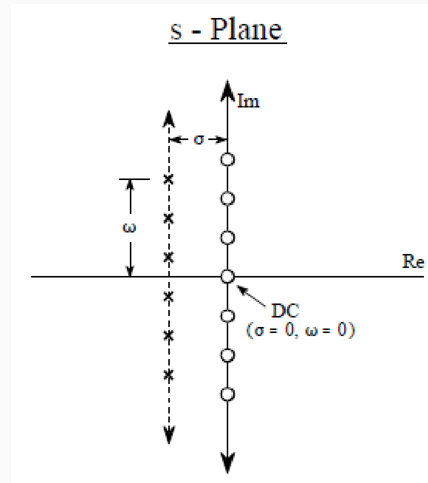
$$q_1 - q_2 = C(v_1 - v_2)$$

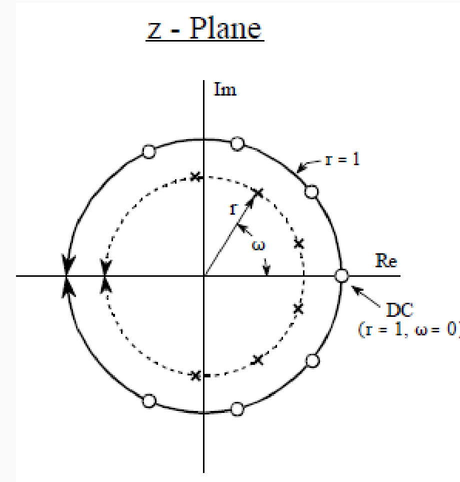
$$I_{avg} = \frac{C(v_1 - v_2)}{T} = \frac{v_1 - v_2}{R_{sc}}$$

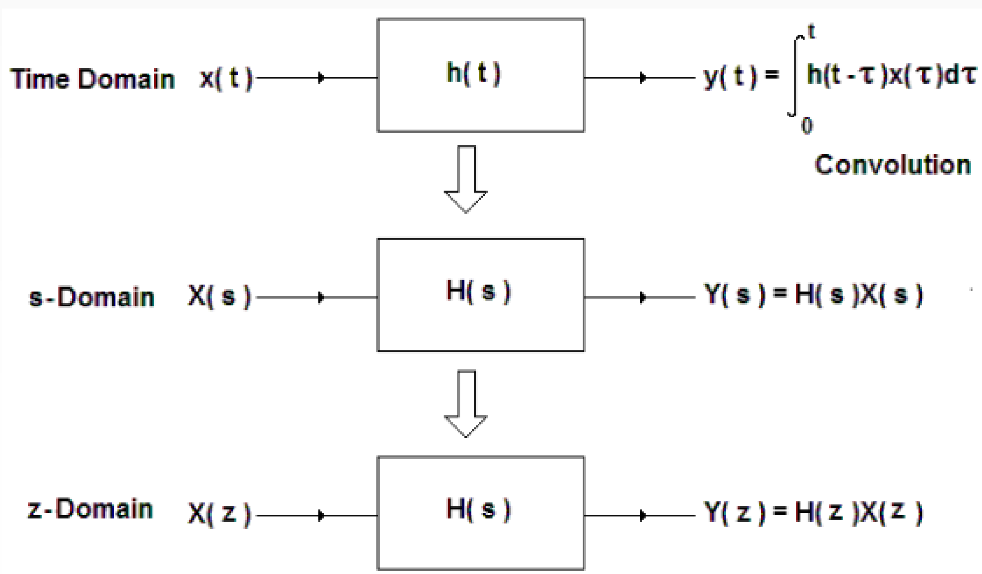
$$\boxed{R_{sc} = \frac{T}{C} = \frac{1}{C \cdot f_{clk}}}$$

Time, S, Z - Domain





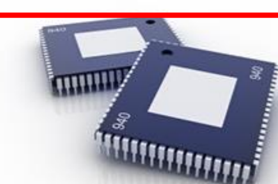




Reference

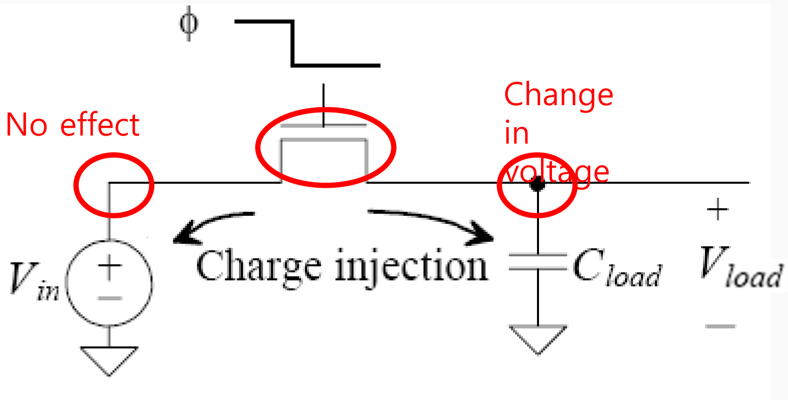
http://www.faqssys.info/replicate-the-fourier-transform-time-frequency-domains-correspondence-illustration-using-tikz/

http://www.analog.com/static/imported-files/tech_docs/dsp_book_Ch33.pdf



Charge-Injection Errors

Charge Injection



Small-signal on-resistance of MOSFET switches

$$Q_I(y) = C'_{ox} \times W \times L \times (V_{GS} - V_{THN})$$

$$\Delta V_{load} = -\frac{C'_{ox} \times W \times L \times (V_{GS} - V_{THN})}{2C_{load}}$$

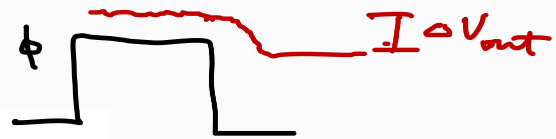
$$\Delta V_{load} = -\frac{C'_{ox} \times W \times L \times (V_{DD} - V_{in} - V_{THN})}{2C_{load}} \quad (10.3)$$

$$\Delta V_{load} = -\frac{C'_{ox} \times W \times L \times \left(V_{DD} - V_{in} - \left[V_{THN0} + \gamma\left(\sqrt{|2V_{fp} - V_{in}|} - \sqrt{|2V_{fp}|}\right)\right]\right)}{2C_{load}}$$

V_{LOAD} is **nonlinear** with respect to V_{in} due to threshold voltage

Minimizing Error Due to Charge-Injection

Capacitive Feedthrough



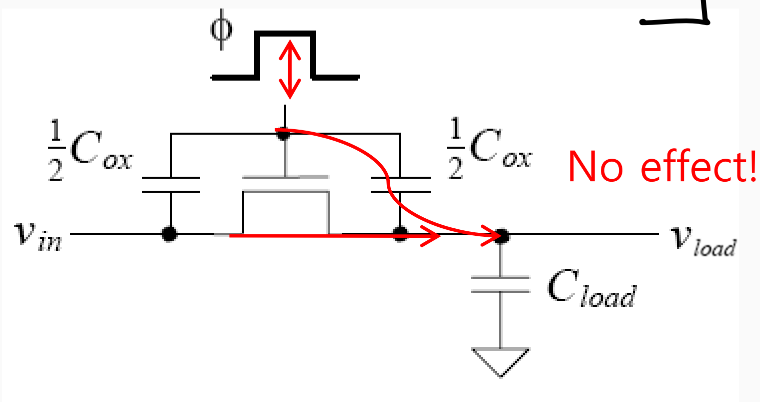


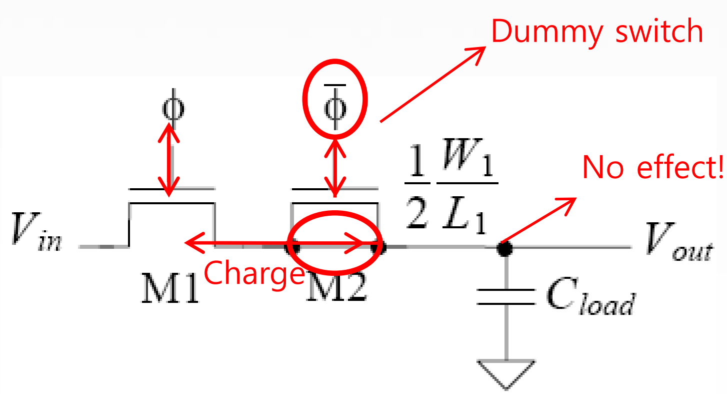
Illustration of capacitive feedthrough

$$C_{overlap} = C'_{ox} \cdot W \cdot LD$$

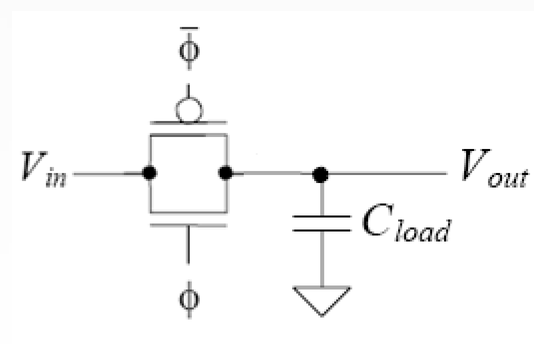
Length of the gate that overlaps the drain/source

$$\Delta v_{load} = \frac{C_{overlap} \cdot VDD}{C_{overlap} + C_{load}} \qquad (10.8)$$

Reduction of Charge Injection and Clock Feedthrough

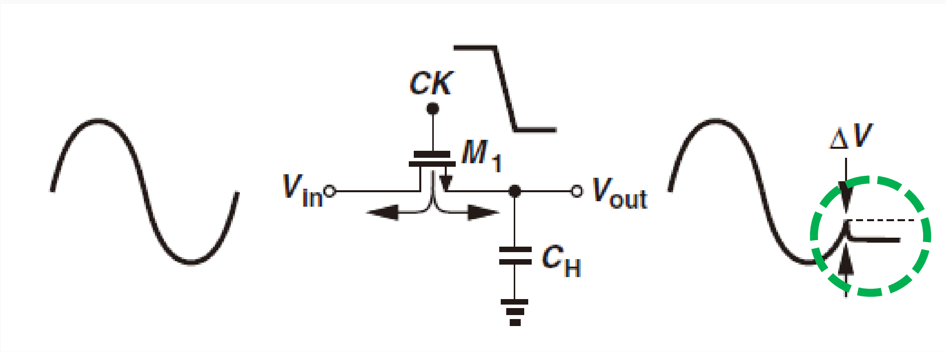


Dummy switch circuit used to minimize charge injection

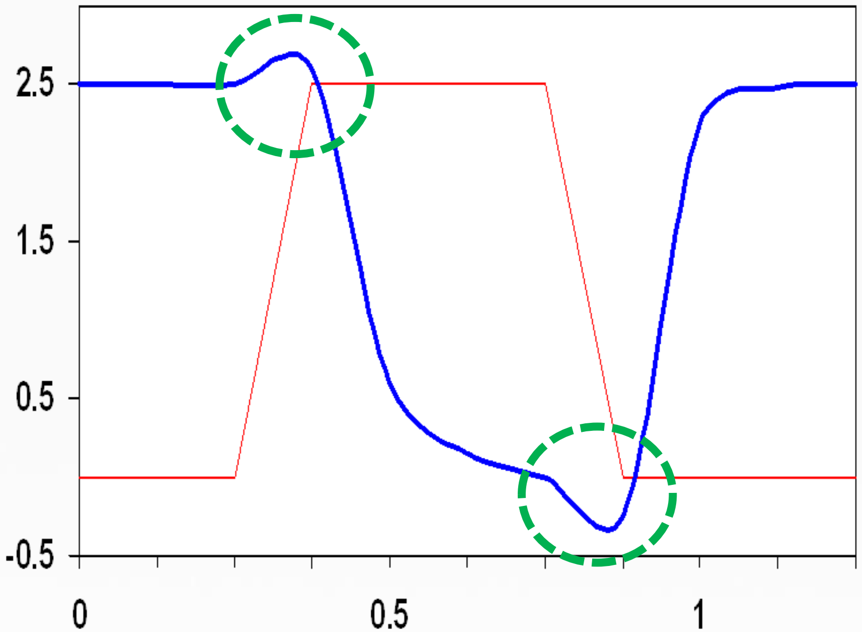


Another method for counteracting charge injection and clock feedthrough

Charge-Injection & Clock Feedthrough



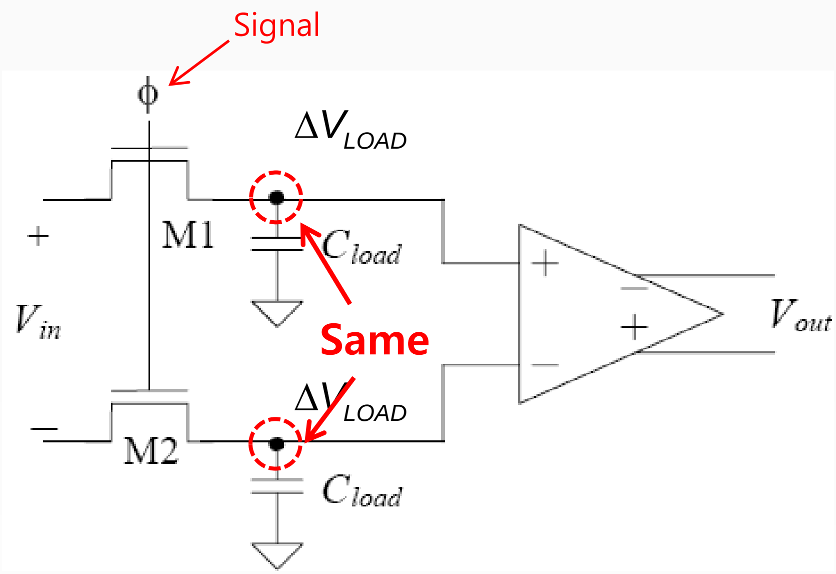
Charge injection



Clock Feedthrough

Minimizing Charge-Injection Error

Reduction of Charge Injection using differential pair



Using a fully-differential circuit to minimize charge injection and clock feedthrough

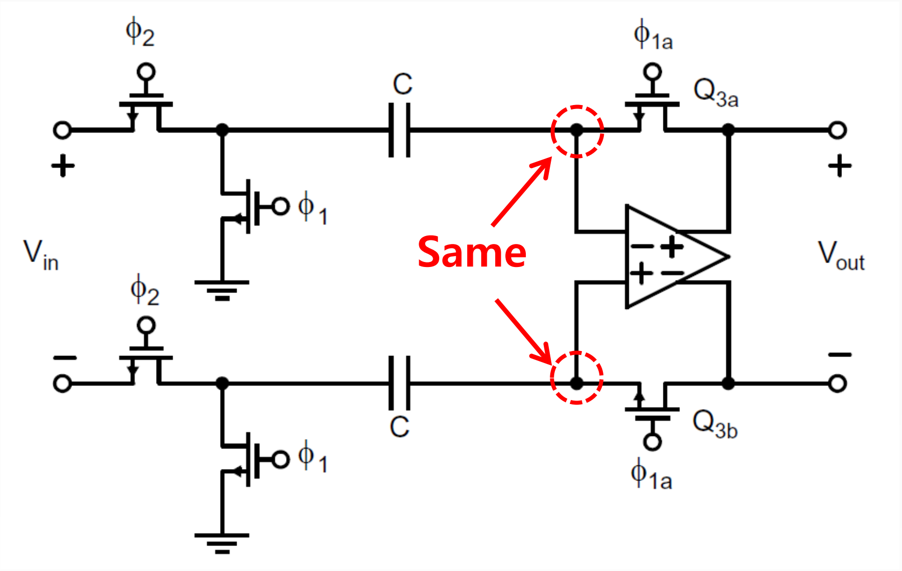
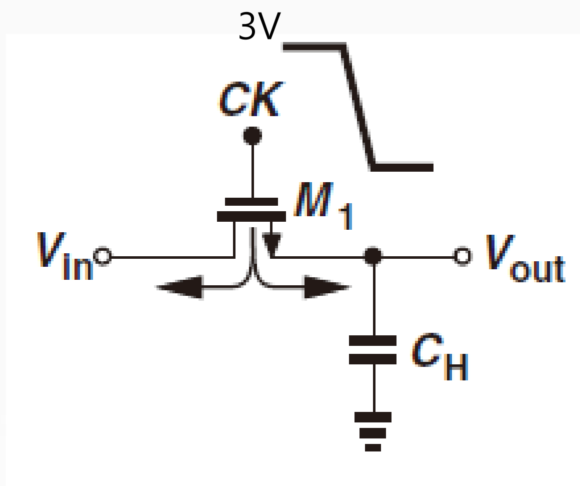


Fig. 10.10 A Fully differential, single-stage, switched-capacitor comparator

Example 1

Parameter values

$$C_H = 1pF,\ C_{ox} = 6.9\,fF/(\mu m)^2,\ (W/L)_1 = 20/0.5,$$
$$C_{OV} = 400p\,F,\ V_{TH} = 0.7V,\ V_{DD} = 3V$$



Charge injection

$$\Delta V = -\frac{(V_{DD}-V_{TH})C_{ox}W_3L_3}{2C} = -\frac{(3-0.7)\times\left(6.9\times10^{-15}/10^{-12}\right)\times10\times10^{-6}\times0.9\times10^{-6}}{2\times1\times10^{-12}}$$
$$= \boxed{-71.415mV}$$

Clock feedthrough

$$C_{ov} = 400p\cdot20\mu = 8fF$$
$$\Delta V'' = -V_{CK}\cdot\frac{C_{ov}}{C_{ov}+C_H} \approx -V_{CK}\cdot\frac{C_{ov}}{C_H} = \frac{8f}{1p}\cdot3V = \boxed{-24mV}$$

Example 2

Parameter values $C = 2pF,\ C_{ox} = 2.1 fF/(\mu m)^2,\ (W/L)_3 = 10\mu m / 0.9\mu m,$
$L_{OV} = 0.1\mu m,\ V_{TH} = 0.8V,\ V_{DD} = 2.6V,\ V_{SS} = -2.6V$

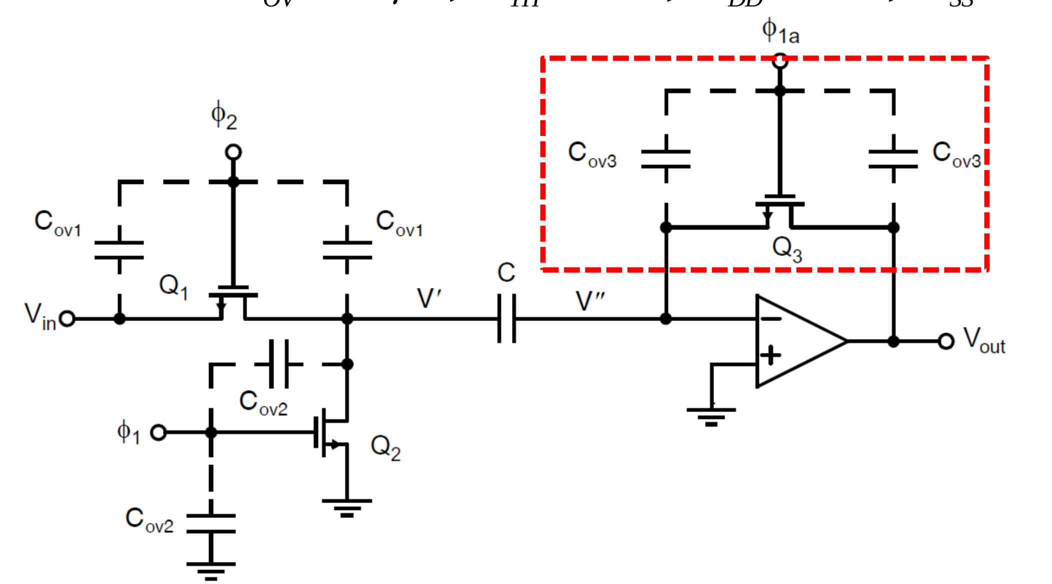


Fig. 10.7 The comparator in Fig. 10.3, with n-channel switches and overlap capacitance shown.

$$\Delta V'' = \frac{(Q_{ch}/2)}{C} \quad (10.3)$$

a. Calculate the voltage change due to channel charge

$$\Delta V'' = -\frac{(V_{DD} - V_{TH})C_{ox}W_3L_3}{2C} = -\frac{(2.6-0.8)\times(2.1\times10^{-3})\times10\times10^{-6}\times0.9\times10^{-6}}{2\times2\times10^{-12}}$$
$$= \boxed{-8.505mV}$$

Example 2(Cont.)

Parameter values

$$C = 2pF,\ C_{ox} = 2.1fF/(\mu m)^2,\ (W/L)_3 = 10\mu m/0.9\mu m,$$
$$L_{OV} = 0.1\mu m,\ V_{TH} = 0.8V,\ V_{DD} = 2.6V,\ V_{SS} = -2.6V$$

b. Calculate the voltage change due to overlap capacitance

Overlap capacitance is given by

$$C_{ov} = W_3 L_{ov} C_{ox} = 10\times10^{-6}\times0.1\times10^{-6}\left(2.1\times10^{-3}\right) = 2.1fF$$

$$\boxed{\Delta V_{load} = \frac{C_{overlap}\cdot VDD}{C_{overlap}+C_{load}}\ (10.8)}$$

Voltage change due to overlap capacitance

$$\Delta V'' = -\frac{(V_{DD}-V_{SS})C_{ov}}{C_{ov}+C} = -\frac{(2.6+2.6)\times2.1\times10^{-15}}{2.1\times10^{-15}+2.1\times10^{-12}} = \boxed{-5.454mV}$$

c. Calculate the total voltage change due to both

$$\Delta V' = -(8.505+5.454)mV = \boxed{-13.959mV}$$