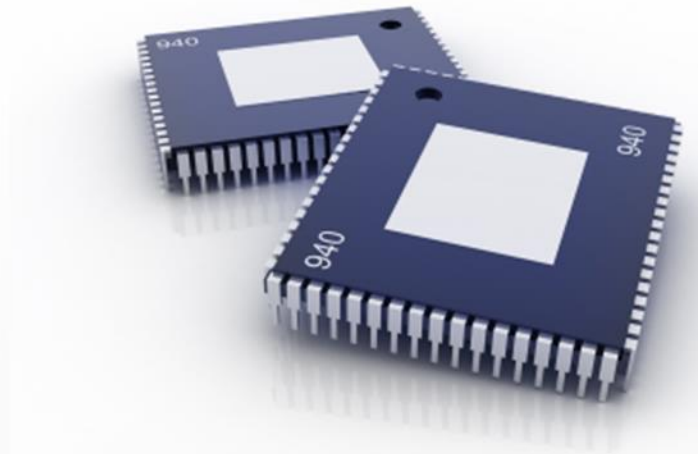



# LECTURE 7

**Soo-Won Kim**

**swkim@korea.ac.kr**

# 7. Biasing, references, and regulators

## 7.1 Analog Integrated Circuit Biasing

## 7.2 Biasing Circuit

## 7.3 Reference Circuit

## 7.4 Voltage Regulator

# Subcircuits

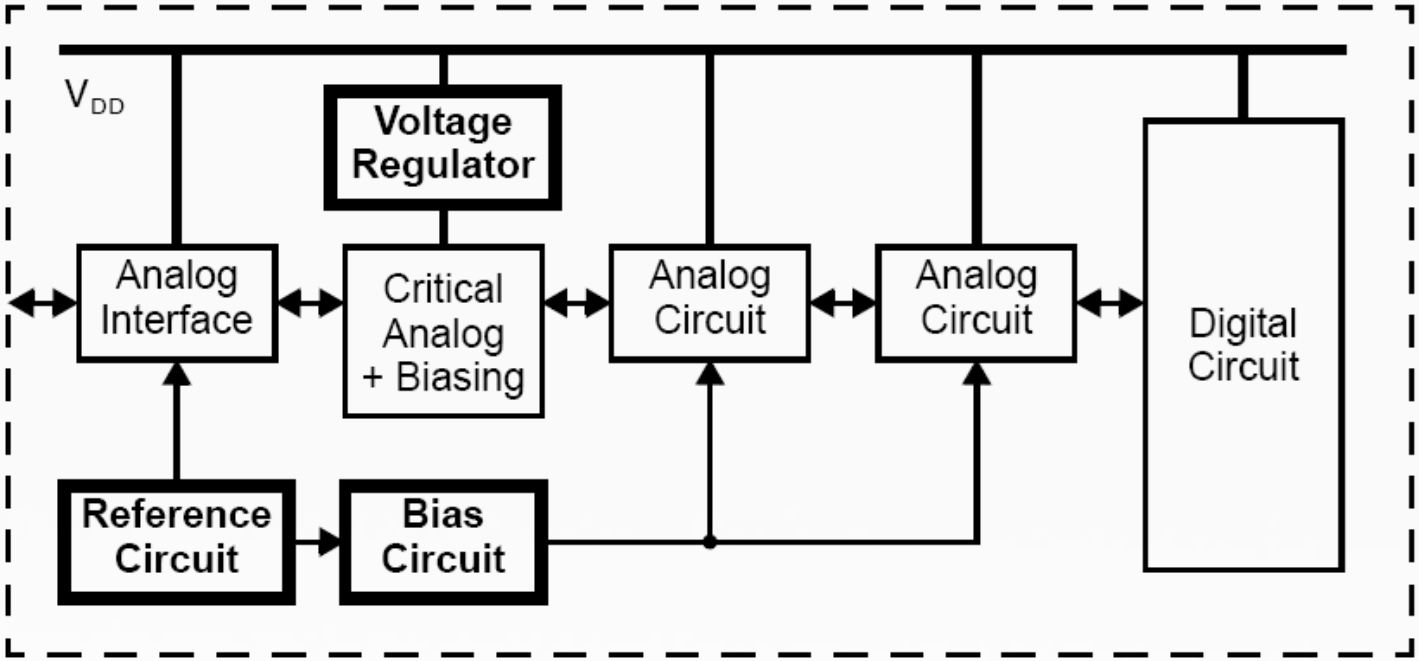
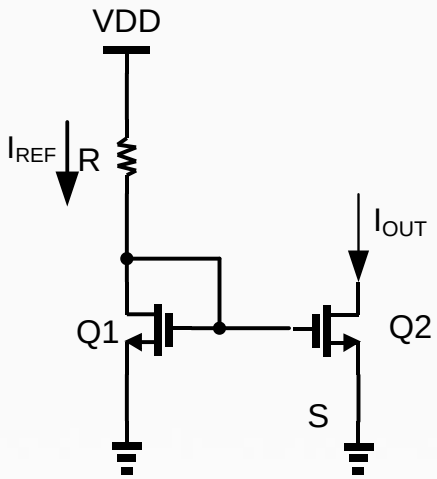


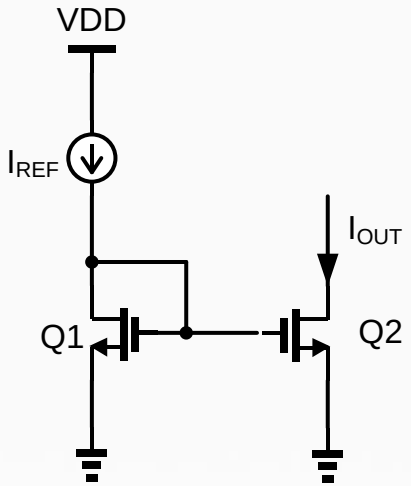

**Fig 7.1 A large mixed analog-digital integrated circuit emphasizing the role of biasing, references, and regulators**

- **Bias circuit** : generates the dc voltages to keep desired operating point
- **Reference circuit** : generates fixed absolute values (voltage or current)
- **Voltage regulator circuit** : improves the quality of a dc voltage or current (decreasing the noise)

# Basic constant-transconductance circuit

## *A basic current mirror*




***When $V_{DD}$ is swept, $V_{GS}$ varies together.***

***Even though $V_{DD}$ is swept, $V_{GS}$ stays***

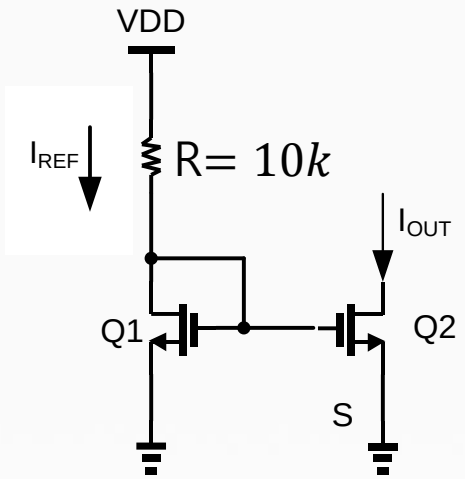
***$I_{OUT}$ is dependent on supply voltage***

***$I_{OUT}$ is independent on supply voltage***

***How do we generate $I_{REF}$ that is independent on $V_{DD}$?***

# Example

a) $V_{DD} = 5V, \mu_n C_{ox} = 200\,\mu/V^2, V_{TH} = 0.7V, (\frac{W}{L})_1 = 10$ 일 때, $V_{GS1}$ 값을 구하여라.




$$I_D = \frac{V_{DD} - V_{GS1}}{R} = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})(V_{GS1} - V_{TH})^2$$

$$V_{GS1} = V_{TH} + \frac{1}{\mu_n C_{ox}(\frac{W}{L}) \cdot R}\left[\sqrt{2(V_{DD} - V_{TH})\mu_n C_{ox}(\frac{W}{L}) + 1} - 1\right]$$

$$= 1.3V$$

b) $V_{DD} = 5.5V$ 일 때, $V_{GS1}$ 값을 구하여라.

$$V_{GS1} = 1.34V$$

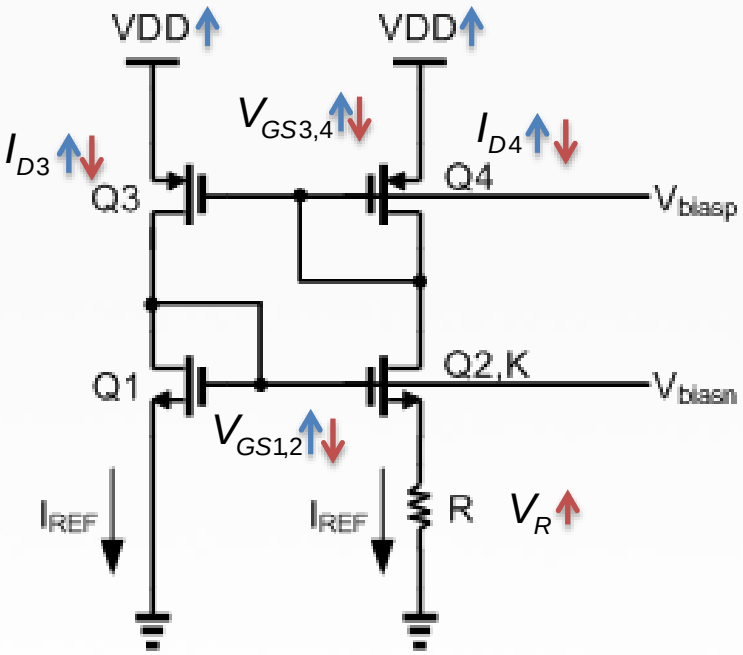
c) R= $11k$ 일 때, $V_{GS1}$ 값을 구하여라.

$$V_{GS1} = 1.33V$$

# Basic constant-transconductance circuit

## *Supply Independent Biasing*

(neglecting channel-length modulation)




$$V_{GS1} = V_{GS2} + I_{REF} \cdot R$$

$$\left( V_{GS} = \sqrt{\frac{2I_{REF}}{\mu_n C_{ox} \cdot \frac{W}{L}}} + V_{THN} \right)$$

$$\sqrt{\frac{2I_{REF}}{\mu_n C_{ox} \cdot \left(\frac{W}{L}\right)_1}} + V_{THN} = \sqrt{\frac{2I_{REF}}{\mu_n C_{ox} \cdot \left(\frac{W}{L}\right)_2}} + V_{THN} + I_{REF} \cdot R$$

$$if \;\; W_2 = K \cdot W_1 \qquad I_{REF} = \frac{2}{R^2 \mu_n C_{ox} \cdot \frac{W_1}{L_1}} \left(1 - \frac{1}{\sqrt{K}}\right)^2$$

⇨ Independent of VDD

$I_{REF}$ is independent from VDD

# Basic constant-transconductance circuit

## *Improved constant-transconductance circuits*

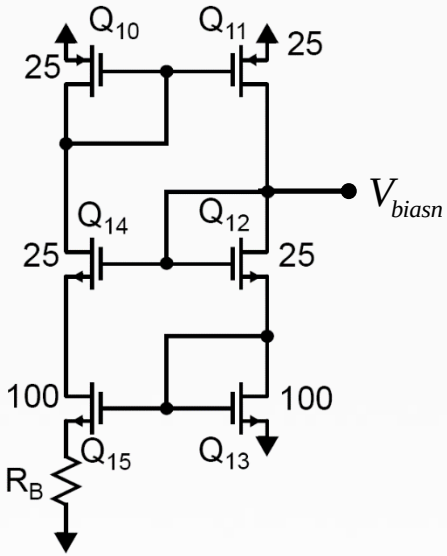



**Fig. 7.6 A bias circuit that gives very predictable and stable transistor transconductances, especially for n-channel devices**

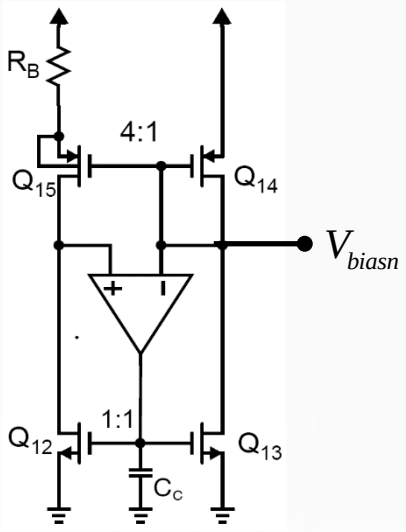



**Fig. 7.7 A modified bias circuit for giving predictable and stable transistor transconductances**

**By cascoding the current mirror**

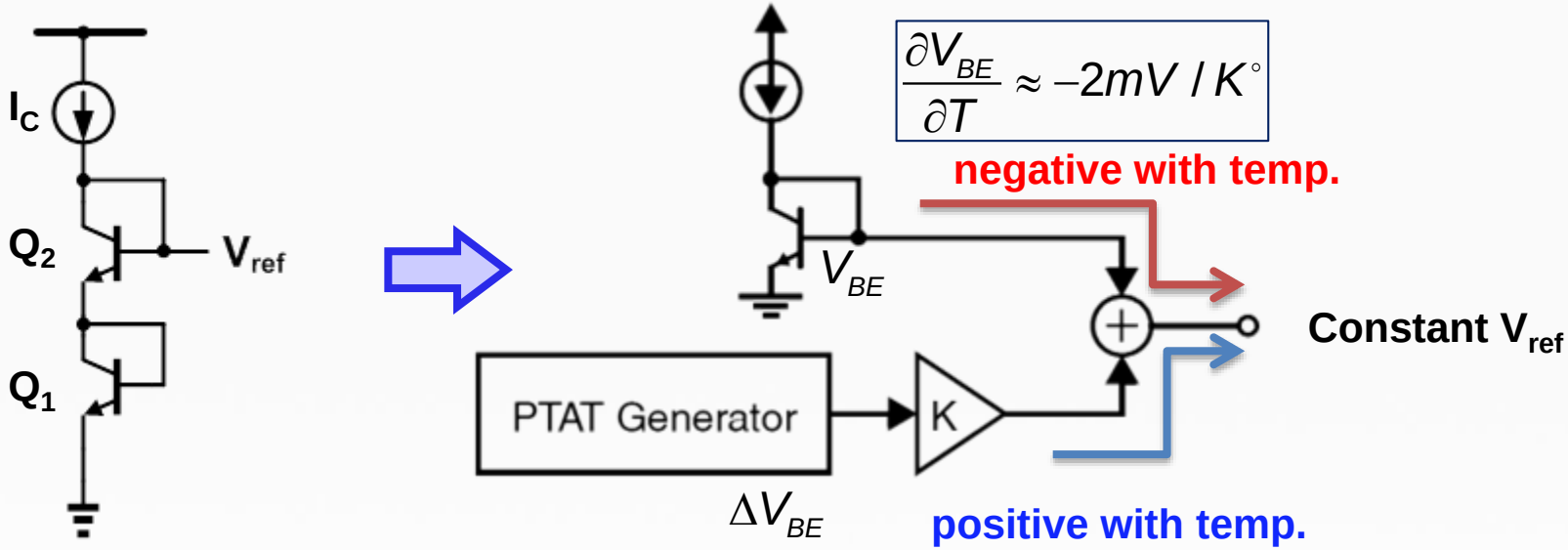
- Current can be made more **equal**
- **Sensitivity** to VDD can be reduced
- Minimum allowable **VDD increases**

**By amplifier the current mirror**

- Minimum allowable **VDD** reduced
- **Stability issue**

# Bandgap Voltage Reference Basics

***Why we use bandgap reference?***




$$V_{ref} = V_{BE1} + V_{BE2}$$

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \Rightarrow V_{BE} = V_T \cdot \ln\left(\frac{I_C}{I_S}\right)$$

**Fig. 7.9 A simplified circuit of a bandgap voltage reference**

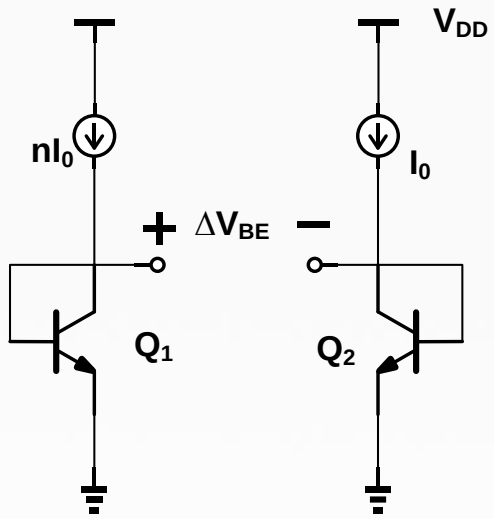
$$V_{ref} = V_{BE} + K\Delta V_{BE}$$

**negative temp. coefficient**

**We can obtain constant voltage**

# Bandgap Voltage Reference Basics

## *Positive-Temperature Coefficient Voltage ($\Delta V_{BE}$)*




$$\Delta V_{BE} = V_{BE1} - V_{BE2}$$
$$= V_T \ln \frac{nI_0}{I_S} - V_T \ln \frac{I_0}{I_S}$$
$$= V_T \ln n = \frac{kT}{q} \ln n$$

$$\boxed{\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln n}$$ **Positive-TC**

$q = 1.6 \times 10^{-19} C,\ k = 1.38 \times 10^{-23} J / {}^{\circ}K$

*Ex ) when n=8, Positive-TC*

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}} \ln 8 = \boxed{0.179 mV / K^{\circ}}$$

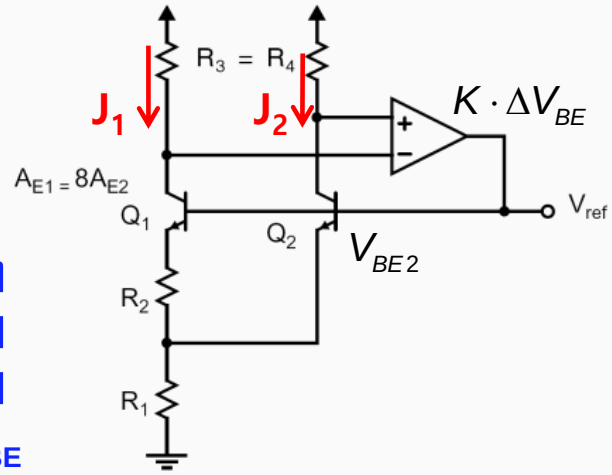
$$V_{ref} = V_{BE} + K \Delta V_{BE}$$

$-2mV / K^{\circ}$

K=10 일 때, $V_{ref}$ 는 일정

# Bandgap Voltage Reference Basics

## *Reference Volatege ($V_{ref}$)*




$$V_{ref} = V_{BE2} + K\Delta V_{BE}$$
$$= V_{G0} + \frac{T}{T_0}(V_{BE0-2} - V_{G0}) + (m-1)\frac{kT}{q}\ln(\frac{T_0}{T}) + K\frac{kT}{q}\ln(\frac{J_2}{J_1})$$

$V_{BE2}$ $\Delta V_{BE}$

$$\frac{\partial V_{ref}}{\partial T} = \frac{1}{T_0}(V_{BE0-2} - V_{G0}) + K\frac{k}{q}\ln(\frac{J_2}{J_1}) + (m-1)\frac{k}{q}[\ln(\frac{T_0}{T}) - 1] = 0$$

**If $T=T_0$,**

$$V_{BE0-2} + K\frac{kT_0}{q}\ln(\frac{J_2}{J_1}) = V_{G0} + (m-1)\frac{kT_0}{q}$$

$$V_{ref-0} = V_{G0} + (m-1)\frac{kT_0}{q}$$

at $q = 1.6\times10^{-19}C$, $k = 1.38\times10^{-23}J/°K$
$m = 2.3, T_0 = 300K, V_{G0} \approx 1.206$

$$V_{ref-0} = 1.24V$$

**Constant $V_{ref}$**

# Example

Determine the ratio of the current density required to get a $\Delta V_{BE}$=59.5mV at room temperature (300K).

**Temperature 300K → 303K, $\Delta V_{BE}$ =59.5mV → $\Delta V_{BE}$ ?**

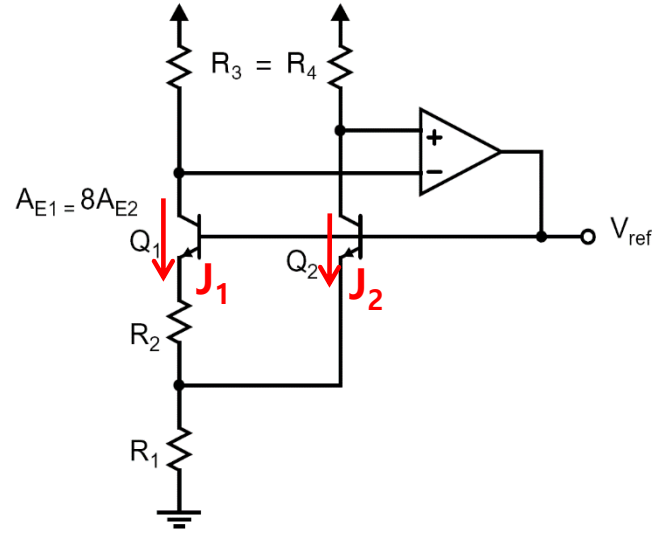



**Fig. 7.10 Band-gap reference**

$$\Delta V_{BE} = \frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right)$$

$$\ln\left(\frac{J_2}{J_1}\right) = \frac{\Delta V_{BE}}{kT/q} = \frac{59.5\times10^{-3}}{1.38\times10^{-23}\times300/1.6.\times10^{-19}} = 2.30$$

$$\frac{J_2}{J_1} = 9.97 \approx 10$$

$$\Delta V_{BE}^{'} = \Delta V_{BE}\frac{T_2}{T_1} = 59.5mV\times\frac{303}{300} = 60.1mV$$

$$59.5mV/300K \text{ or } 0.198mV/K$$

# Circuits for Bandgap References

## *Bipolar Bandgap References*

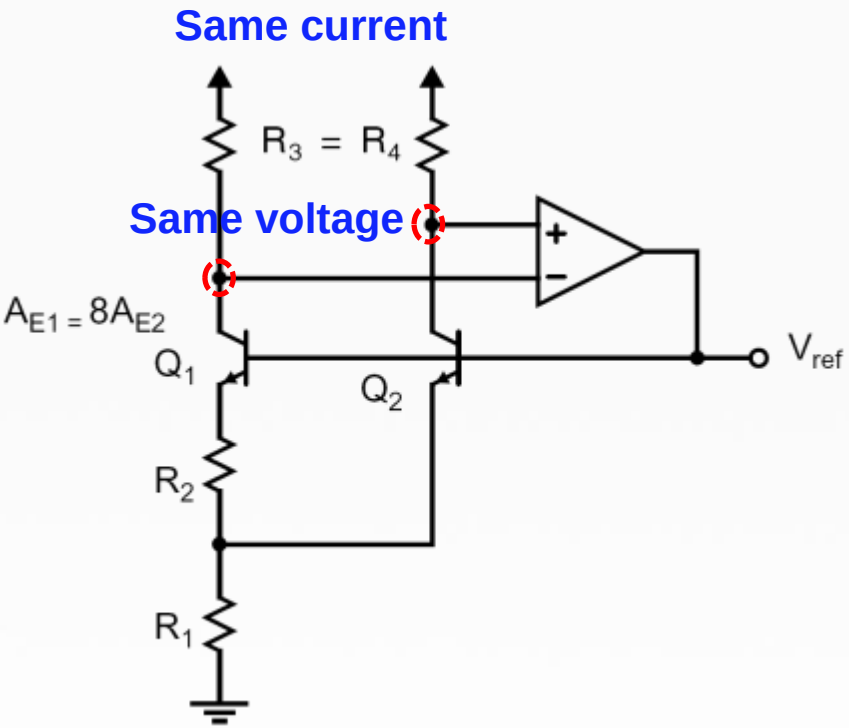
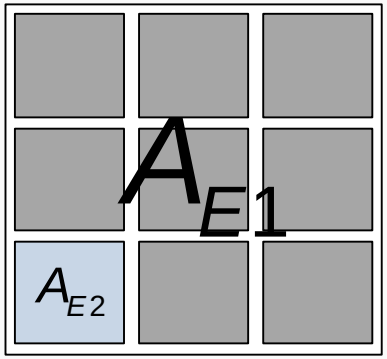



**Fig. 7.10 A simplified schematic of a bipolar bandgap voltage reference**

***cf) why $A_{E1}=8A_{E2}$ ?***




$$V_{ref} = V_{BE2} + V_{R1}$$

$$V_{R1} = I_{R1}R_1 = 2I_{R2}R_1$$

$$I_{R_2} = \frac{V_{R2}}{R_2} = \frac{V_{BE2} - V_{BE1}}{R_2} = \frac{\Delta V_{BE}}{R_2}$$

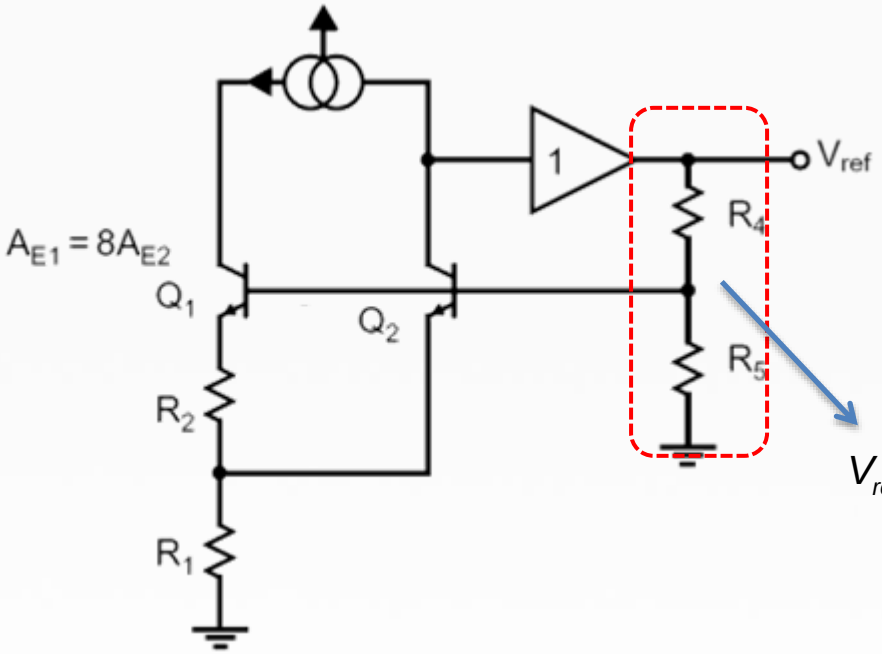
$$V_{ref} = V_{BE2} + \frac{2R_1}{R_2}\Delta V_{BE}$$

Negative Positive

***Constant 1.24V***

# Circuits for Bandgap References

## *Case 1) How to get high reference voltages (> 1.26V)*




**larger voltage than 1.24V**

$$V_{ref} = \left(1 + \frac{R_4}{R_5}\right) \cdot 1.24V$$

**Voltage at this node**

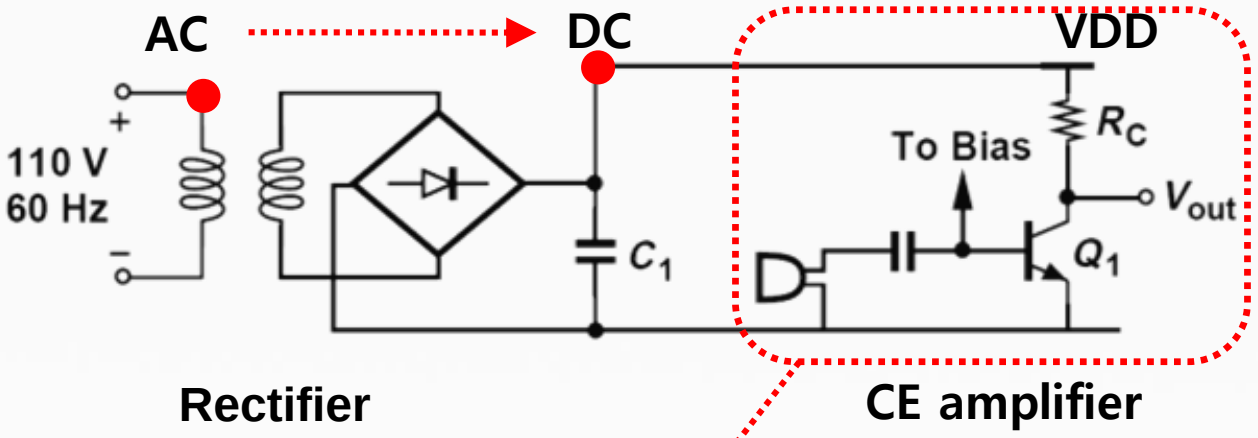
$$V_{ref}' = V_{BE2} + \frac{2R_1}{R_2}\Delta V_{BE} \approx 1.24V$$

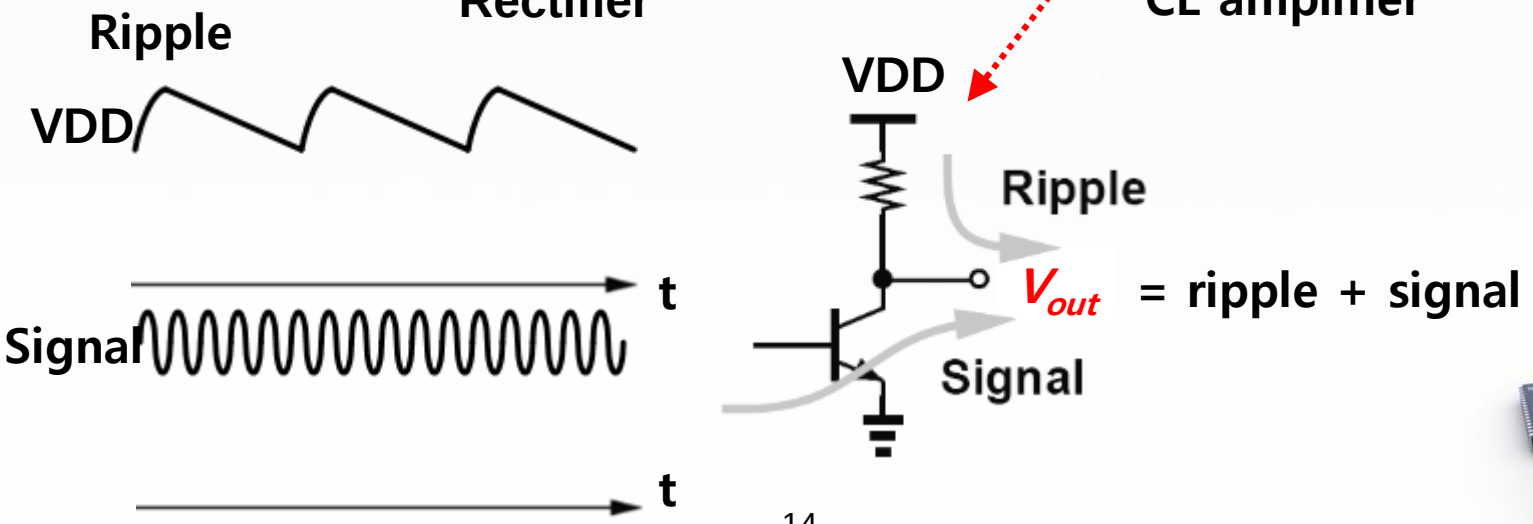
**Fig. 7.11 A bipolar bandgap with output voltages greater than 1.26V**

# Ripple Voltage

***Problem***

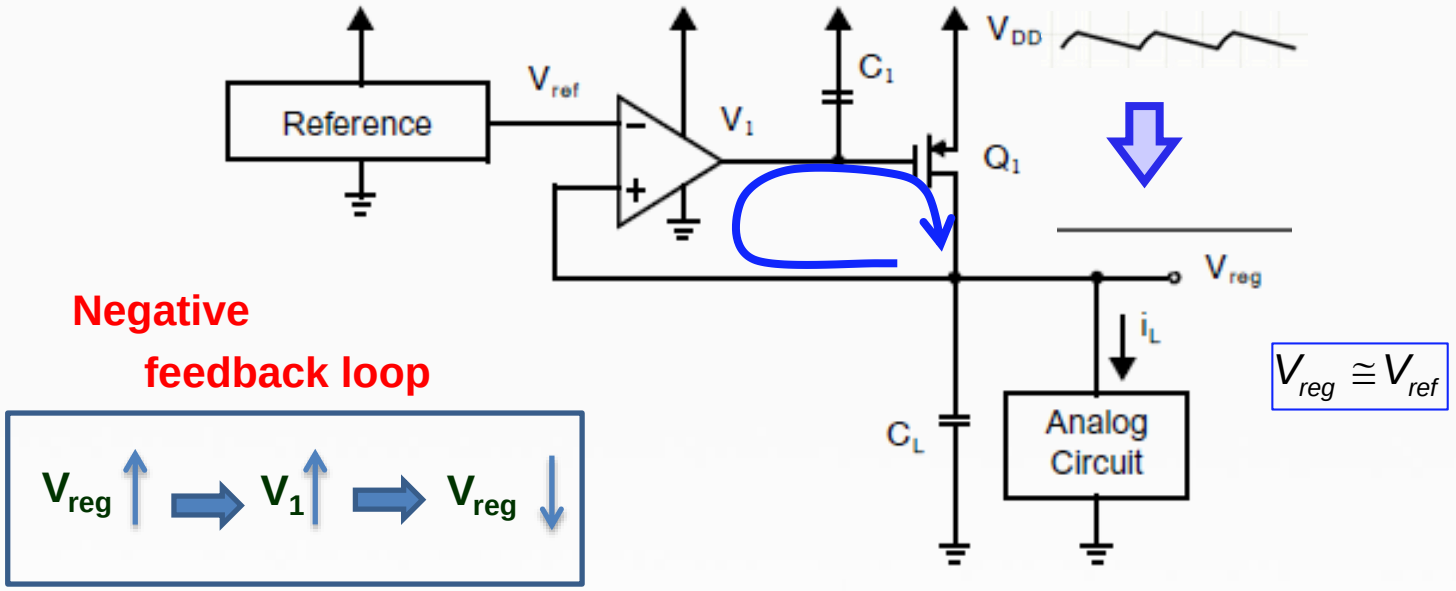
1) $V_{DD}$ contains ripple
2) Analog circuit needs the accurate DC voltage



# Voltage Regulator

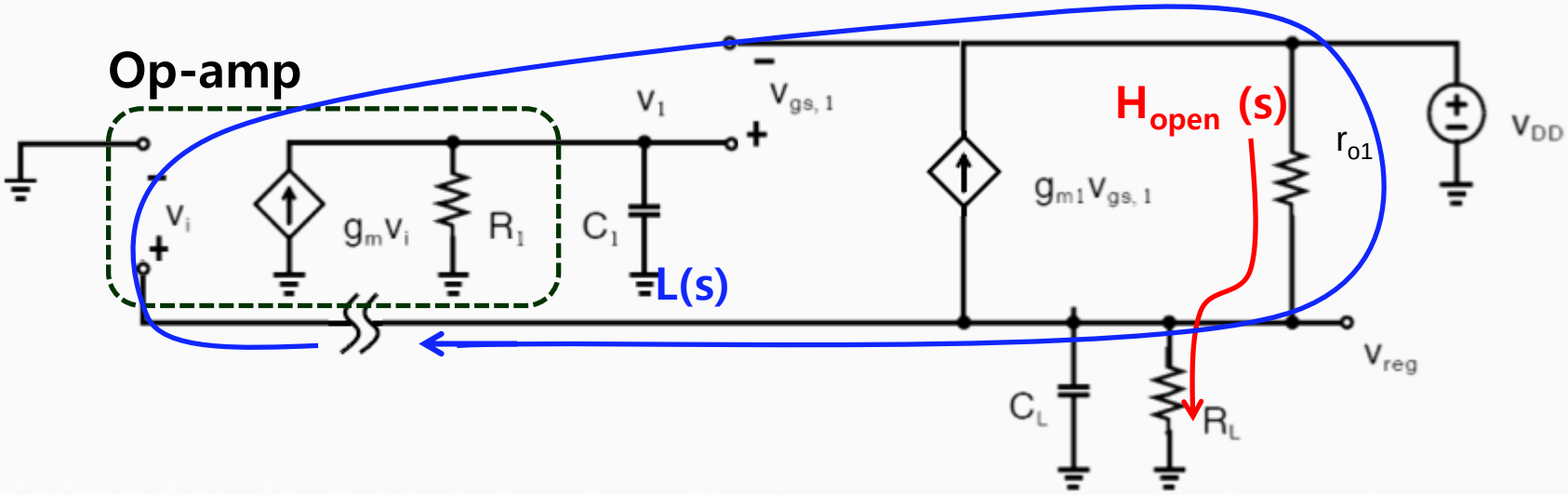
***How to eliminate the ripple?***




- **Power Supply Rejection Ratio(PSRR) : how well the noise of $v_{reg}$ is regulated from the noise of $v_{dd}$**

$$PSRR(\omega) = \frac{V_{dd}}{V_{reg}}(\omega)$$

# Small signal analysis




**$v_{reg}/v_{dd}$ open-loop gain,**

$$H_{open}(s)=\left(\frac{R_L}{R_L+r_{o1}}\right)\cdot\frac{1}{1+sR_LC_L}$$

**Loop gain, L(s)**

$$L(s)=\frac{A_V\cdot g_{m1}\cdot\left(R_L\|r_{o1}\right)}{\left(1+sR_1C_1\right)\cdot\left(1+sC_L\left(R_L\|r_{o1}\right)\right)}$$

**$v_{reg}/v_{dd}$ closed-loop gain,**

$$H_{closed}(s)=\frac{v_{reg}}{v_{dd}}(s)=\frac{H_{open}}{1+L(s)}=PSRR^{-1}(\omega)$$

# $v_{reg}/v_{dd}$ ($PSRR^{-1}$)

## *Transfer function of $PSRR^{-1}$*

$$PSRR^{-1}(\omega) = \frac{v_{reg}}{v_{dd}}(s) = \frac{H_{open}}{1+L(s)} \qquad H_{open}(s) = \left(\frac{R_L}{R_L + r_{o1}}\right) \cdot \frac{1}{1+sR_LC_L}$$

⇒ **One pole**

$$\frac{1}{1+L(s)} = \frac{1}{1+\dfrac{A_v g_{m1}(R_L \,||\, r_{o1})}{(1+sR_1C_1)(1+sC_L(R_L \,||\, r_{o1}))}}$$

$$= \frac{(1+sR_1C_1)(1+sC_L(R_L \,||\, r_{o1}))}{1+A_v g_{m1}(R_L \,||\, r_{o1}) + s(R_1C_1 + C_L(R_L \,||\, r_{o1})) + s^2R_1(R_L \,||\, r_{o1})C_1C_L}$$

**Using dominant pole approximation,**

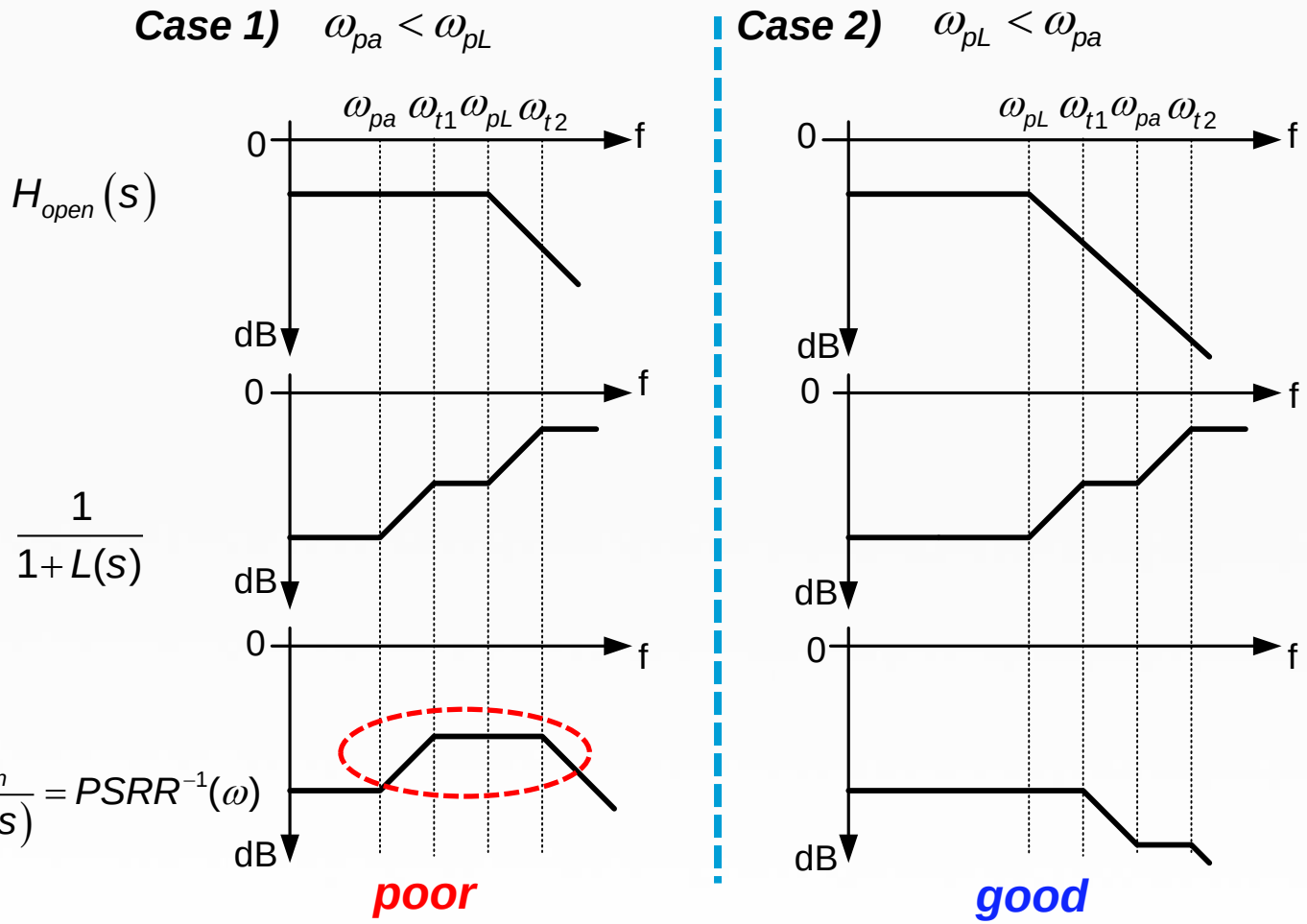
**(분모)** → $1 + s\underbrace{\dfrac{R_1C_1 + (R_L \,||\, r_{o1})C_L}{1+A_v g_{m1}(R_L \,||\, r_{o1})}}_{b} + s^2\underbrace{\dfrac{R_1(R_L \,||\, r_{o1})C_1C_L}{1+A_v g_{m1}(R_L \,||\, r_{o1})}}_{a} = 0$

$$\frac{1}{b} = \omega_{t1} = \frac{1+A_v g_{m1}(R_L \,||\, r_{o1})}{R_1C_1 + (R_L \,||\, r_{O1})C_L} = (1+A_v g_{m1}(R_L \,||\, r_{o1}))(\omega_{pa} \,||\, \omega_{pL})$$

$$\frac{b}{a} = \omega_{t2} = \frac{1}{R_1C_1} + \frac{1}{(R_L \,||\, r_{o1})C_L} = \omega_{pa} + \omega_{pL}$$

⇒ **Two *poles* & two *zeros***

# Frequency response in PSRR$^{-1}$




$\omega_{pL} < \omega_{pa}$ **requires high power consumption in the op-amp to keep low $R_1$**

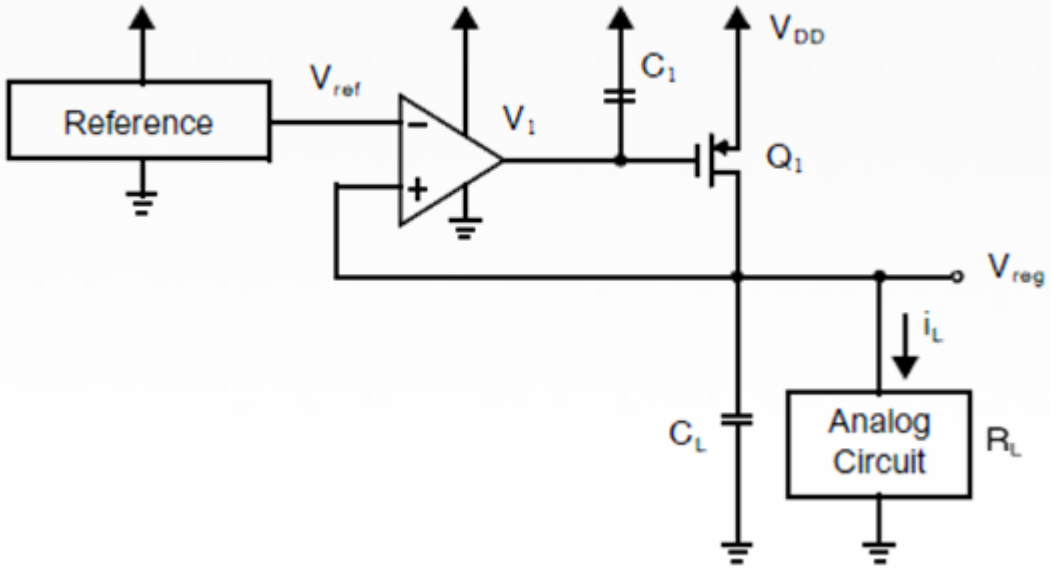
# Example

***The regulator is to be operated with $R_L$=1kΩ, $C_L$=1nF, $C_1$=10pF. The PMOS of regulator delivers 5mA of output current. (Each gain of op-amp and PMOS is 10.)***

a. *Determine the resistance at output node. (λ=0.05)*

b. *Calculate $\omega_{pL}$ and $\omega_{Pa}$ with 1) $R_1$=100MΩ, 2) $R_1$=100Ω*

c. *Sketch PSRR$^{-1}$(ω), 1) $R_1$=100MΩ, 2) $R_1$=100Ω*



# Solution

a. *Determine the resistance at output node.*

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.05 \times 5mA} = 4k\Omega \qquad r_o \,||\, R_L = 4k\Omega \,||\, 1k\Omega = 800\Omega$$

b. *Calculate $\omega_{pL}$ and $\omega_{Pa}$ with 1) $R_1$=100MΩ, 2) $R_1$=100Ω*

$$\omega_{pL} = \frac{1}{(R_L \,||\, r_o)C_L} = \frac{1}{800 \times 10^{-9}} = 1.25MHz$$

$$1)\ \omega_{pa} = \frac{1}{R_1 C_1} = \frac{1}{10^8 \times 10^{-11}} = 1kHz$$

$$2)\ \omega_{pa} = \frac{1}{R_1 C_1} = \frac{1}{10^2 \times 10^{-11}} = 1GHz$$

c. *Sketch PSRR$^{-1}$(ω), 1) $R_1$=100MΩ, 2) $R_1$=100Ω*

$$\omega_{t1} = (1 + A_v g_{m1}(R_L \,||\, r_{o1}))(\omega_{pa} \,||\, \omega_{pL})$$
$$\omega_{t2} = \omega_{pa} + \omega_{pL}$$

$$1)\ \omega_{t1} = 101 \times (1kHz \,||\, 1.25MHz) = 100.9kHz,$$
$$\omega_{t2} = 1.25MHz + 1kHz = 1.251MHz$$

$$2)\ \omega_{t1} = 101 \times (1GHz \,||\, 1.25MHz) = 126MHz$$
$$\omega_{t2} = 1.25MHz + 1GHz = 1.00125GHz$$

# Solution(Cont'd)

*c. Sketch PSRR$^{-1}(\omega)$, 1) $R_1$=100MΩ, 2) $R_1$=100Ω (Cont'd)*