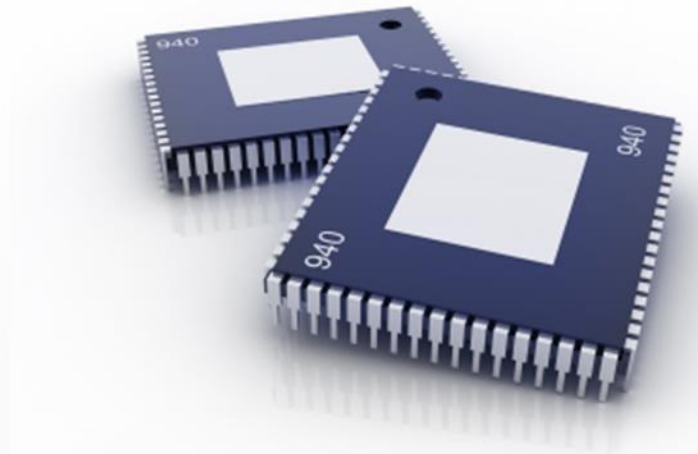

LECTURE 15

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Lecture 15

17. Nyquist-rate A/D converter

17.1 Integrating converters

17.2 Successive-approximation converter

17.3 Algorithmic (or cyclic) A/D converter

17.4 Pipelined A/D converter

17.5 Flash converters

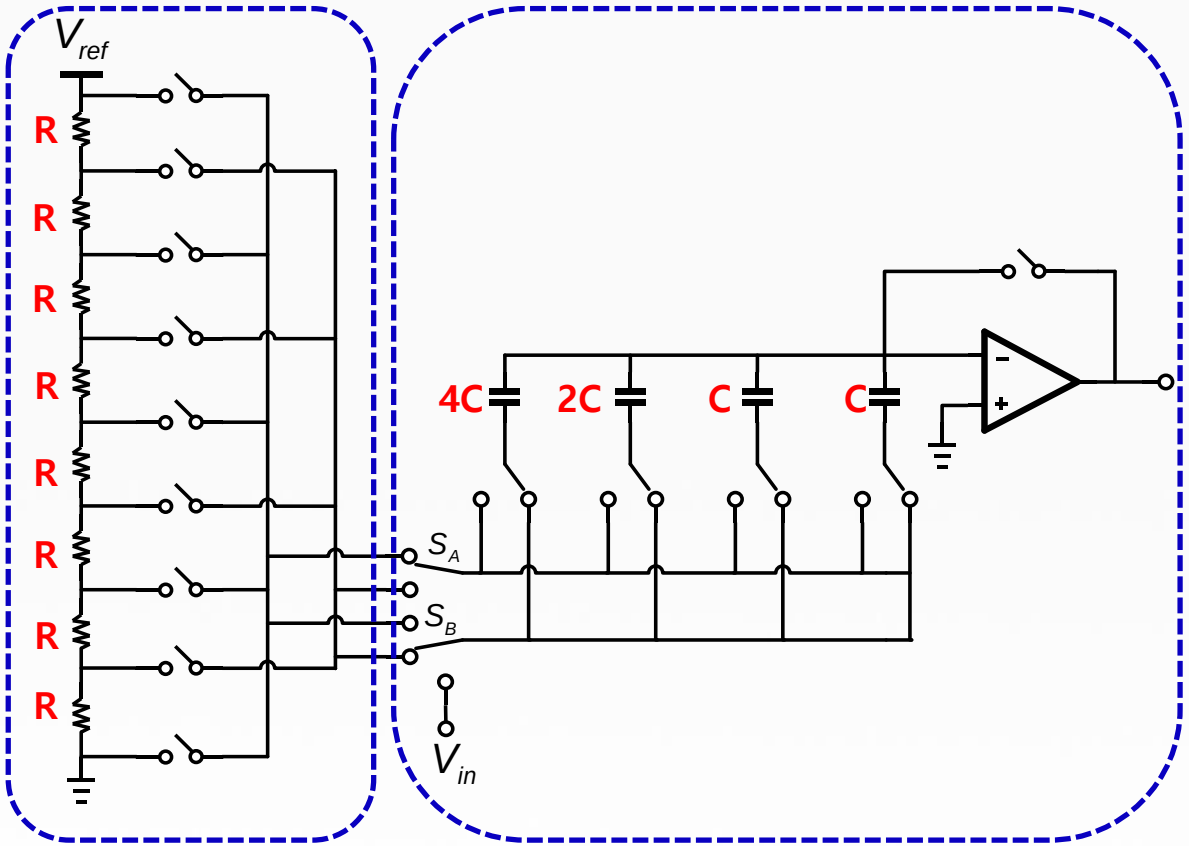
17.6 Two-step A/D converters

17.7 Interpolating A/D converters

17.8 Folding A/D converters

17.9 Time-interleaved A/D converters

Resistor – Capacitor Hybrid(6-bit)



MSB(3-bit)

LSB(3-bit)

Multi-Bit Successive-Approximation

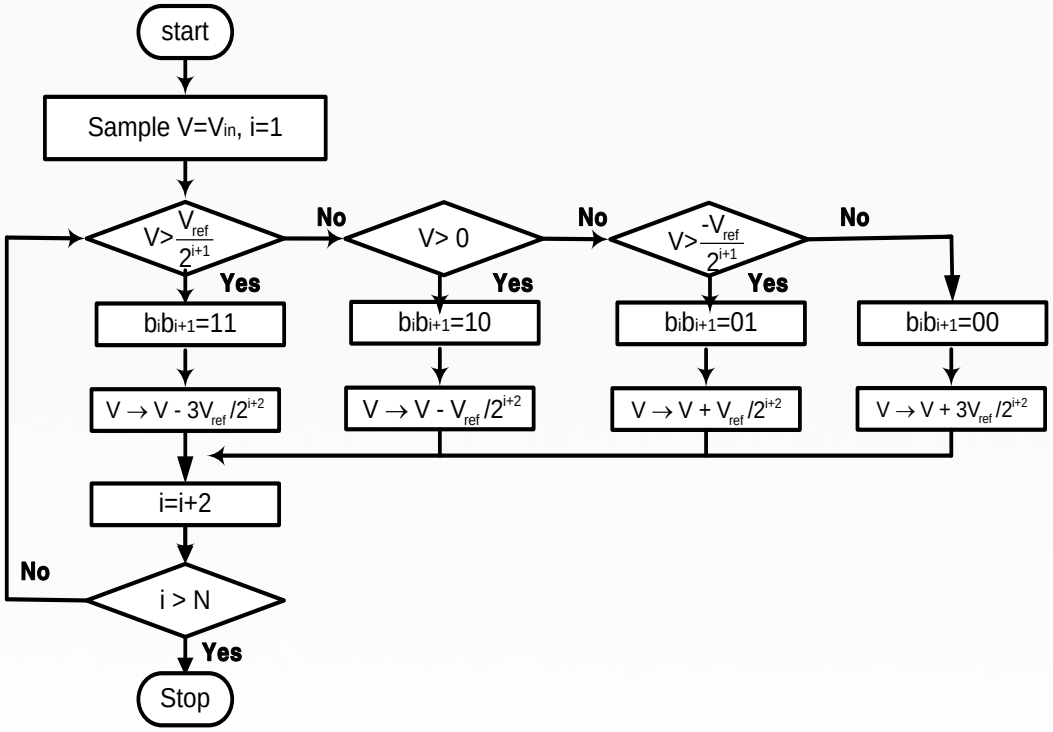
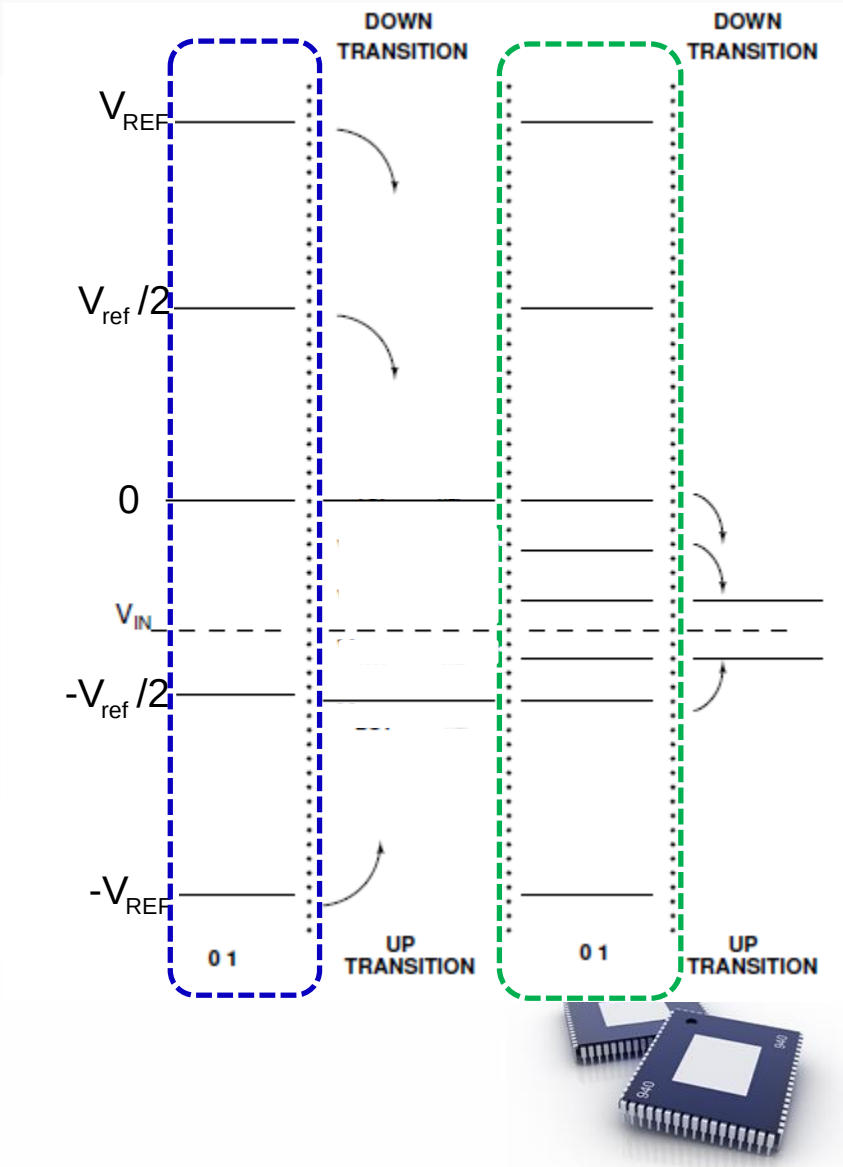
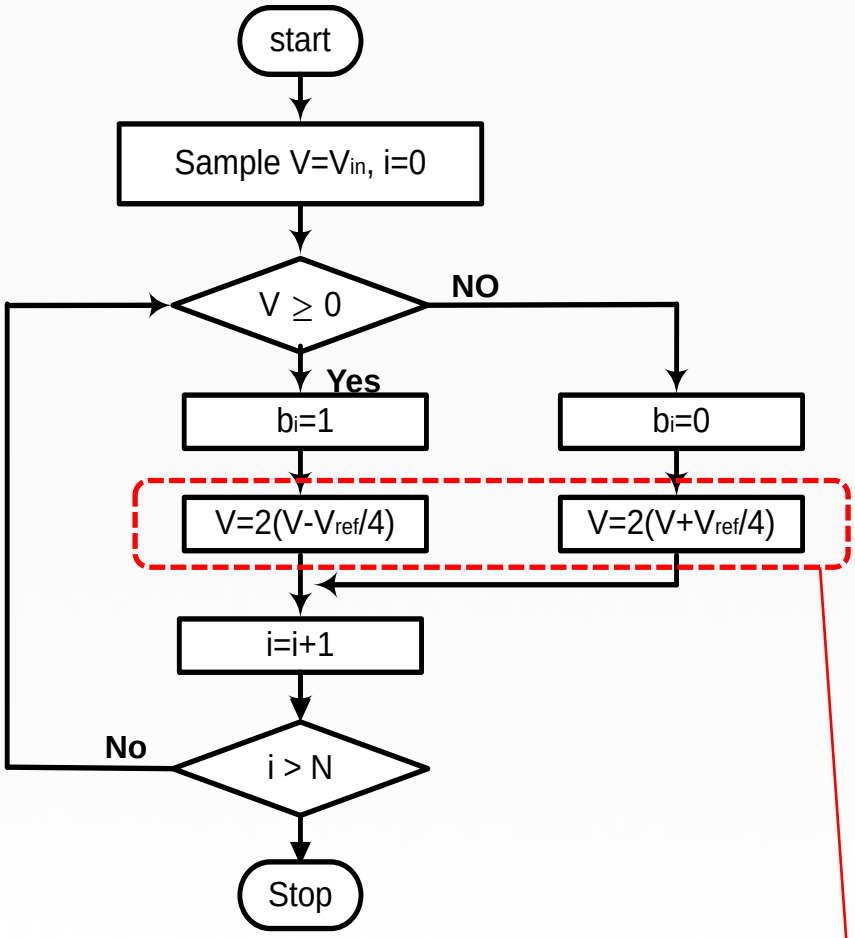


Fig. 17.13 Flow graph for 2-Bit Successive-Approximation

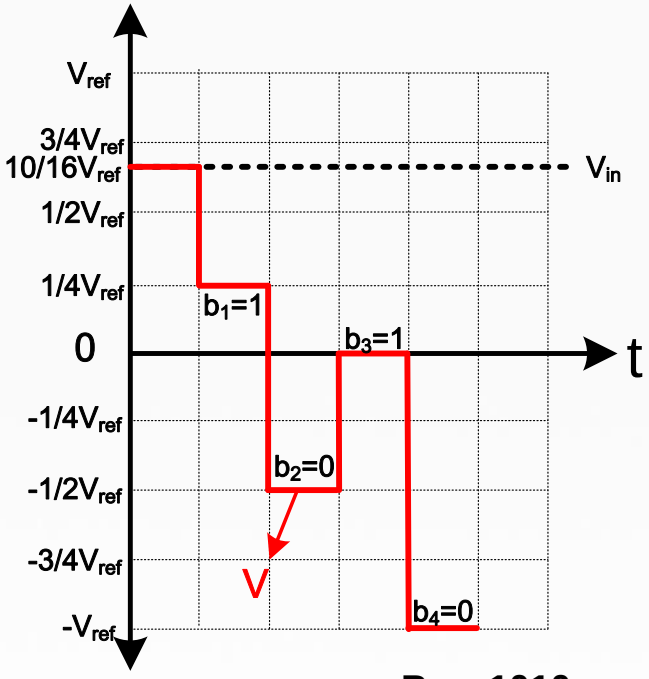


17. Nyquist-rate A/D converter

Basic Operation



Ex) N = 4bit , $V_{in} = \frac{10}{16} V_{ref}$



B_{out}=1010

Fig. 17.14 Flow graph for the algorithmic and pipelined converter approach

$$V_{i+1} = 2[V_i + (b_i - 0.5)V_{ref} / 2]$$

Algorithmic ADC block diagram

Algorithmic converter

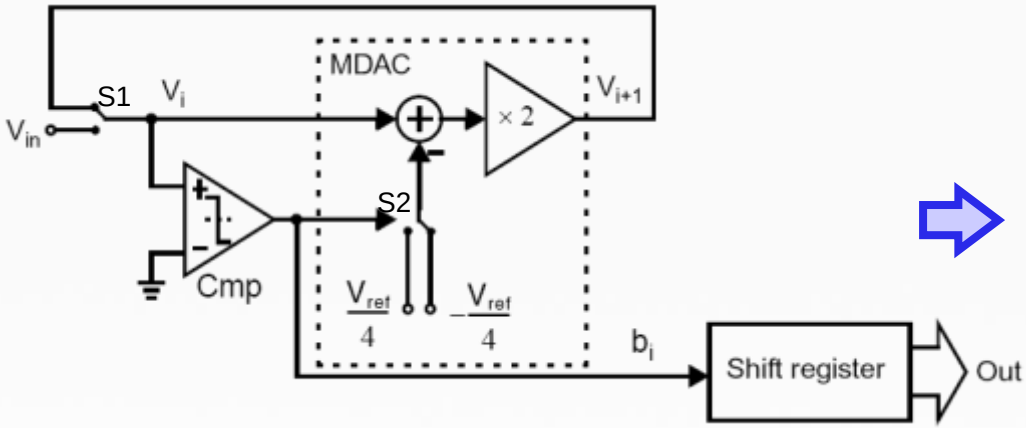
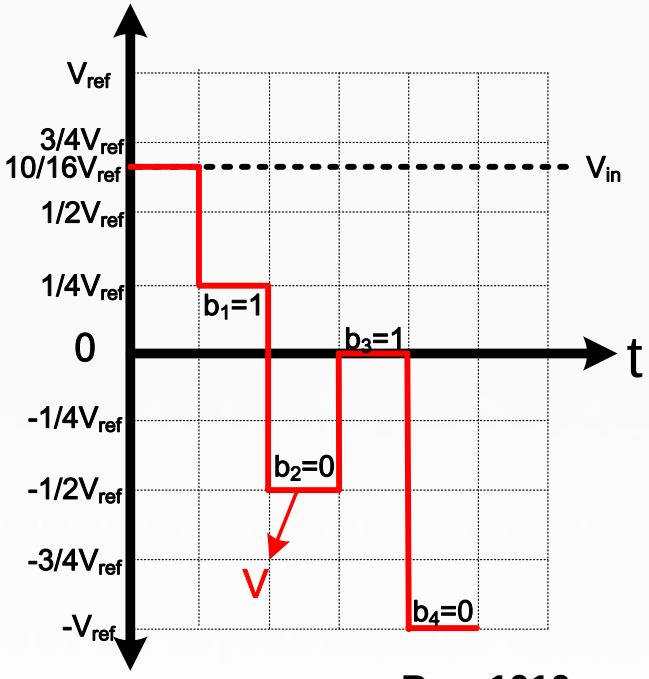


Fig. 17.15 Algorithmic converter

Ex) N = 4bit, $V_{in}=\frac{10}{16}FS$



B_{out}=1010

- Small amount of analog circuitry
- Requires N step for N-bit converter

SAR ADC와 달리, capacitor array & DAC 대신에 2배의 gain 값을 갖는 Amp 사용.

Example 1

Find V_i and b_i(i=1,2,3,4,) during the operation of the 4-bit & 6bit algorithmic (or cyclic) converter. Assume that V_{in} = 1.23V, V_{ref} = 10V.

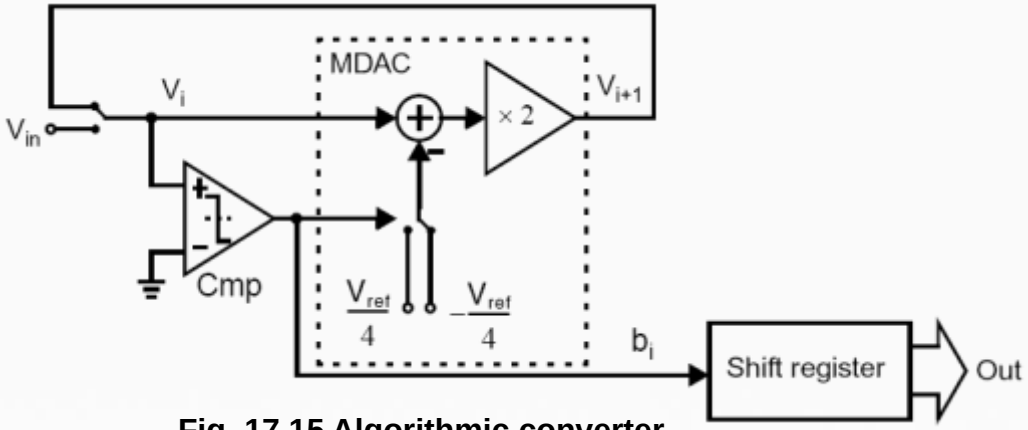
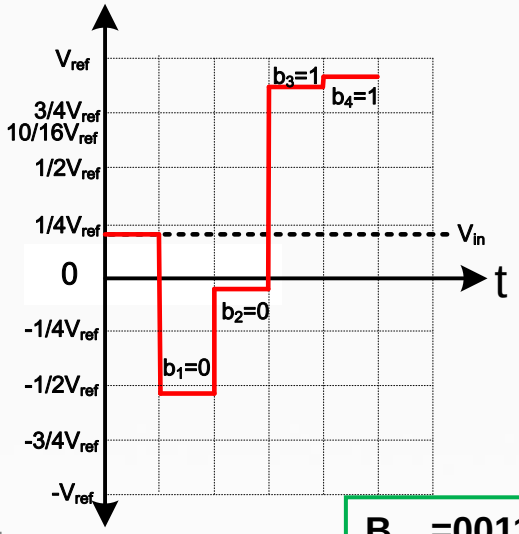


Fig. 17.15 Algorithmic converter



B_{out}=0011

- i = 1

$$V_1 = V_{in} = 1.23V > 0$$
$$\downarrow$$
$$V_1 \rightarrow 2\left(V_1 - \frac{V_{ref}}{4}\right)$$
$$= -2.54 < 0$$
$$\downarrow$$
$$b_1 = 0$$

- i = 2

$$V_2 = -2.54V < 0$$
$$\downarrow$$
$$V_2 \rightarrow 2\left(V_2 + \frac{V_{ref}}{4}\right)$$
$$= -0.08 < 0$$
$$\downarrow$$
$$b_2 = 0$$

- i = 3

$$V_3 = -0.08V < 0$$
$$\downarrow$$
$$V_3 \rightarrow 2\left(V_3 + \frac{V_{ref}}{4}\right)$$
$$= 4.84 > 0$$
$$\downarrow$$
$$b_3 = 1$$

$$V_4 = 4.84V > 0$$
$$\downarrow$$
$$V_4 \rightarrow 2\left(V_4 - \frac{V_{ref}}{4}\right)$$
$$= 4.68 > 0$$
$$\downarrow$$
$$b_4 = 1$$

Example 1(Cont.)

Find V_i and b_i(i=1,2,3,4,) during the operation of the 4-bit & 6bit algorithmic (or cyclic) converter. Assume that V_{in} = 1.23V, V_{ref} = 10V.

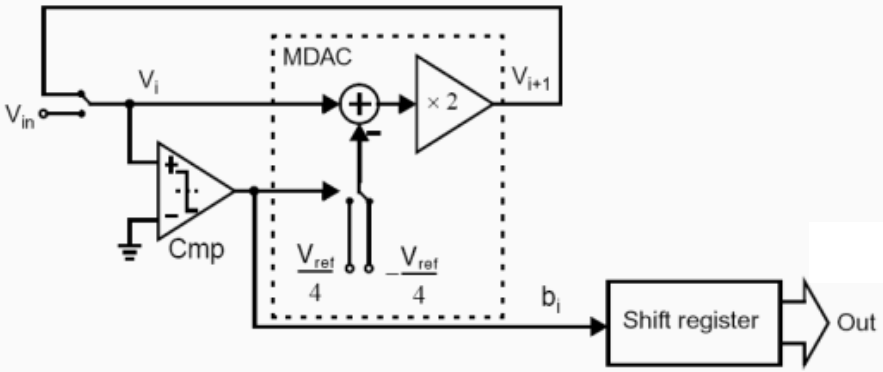


Fig. 17.15 Algorithmic converter

- i = 5

$$V_5 = 4.68V > 0$$

$$\downarrow$$

$$V_5 \rightarrow 2\left(V_5 - \frac{V_{ref}}{4}\right)$$

$$= 4.36 > 0$$

$$\downarrow$$

$$b_5 = 1$$

- i = 6

$$V_4 = 4.36V > 0$$

$$\downarrow$$

$$V_6 \rightarrow 2\left(V_6 - \frac{V_{ref}}{4}\right)$$

$$= 3.72 > 0$$

$$\downarrow$$

$$b_4 = 1$$

- 4bit converter

$$b_i = 0011 \Rightarrow V_{DAC} = \frac{3}{16} \times 5 = 0.9375V$$

0.2345V

- 6bit converter

$$b_i = 001111 \Rightarrow V_{DAC} = \frac{15}{64} \times 5 = 1.172V$$

Example 2

What will happen if the comparator has an offset of 30 mV ?

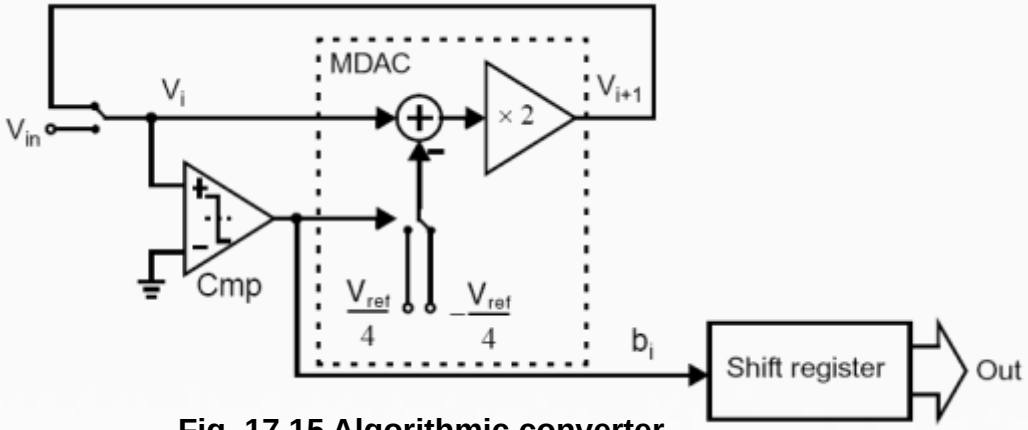
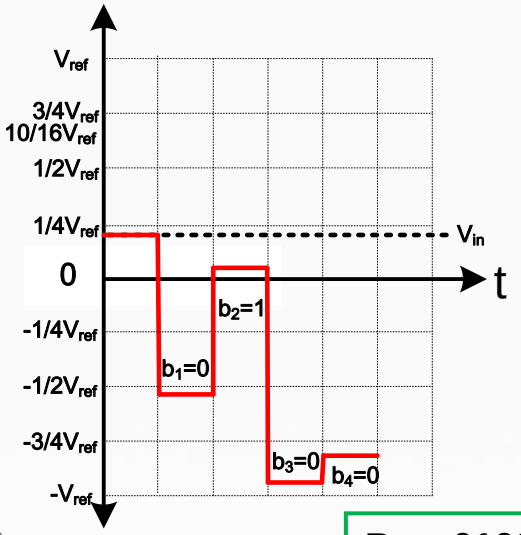


Fig. 17.15 Algorithmic converter



B_{out}=0100

- i = 1

$$V_1 = V_{in} = 1.23V > 0$$

$$\downarrow$$

$$V_1 \rightarrow 2\left(V_1 - \frac{V_{ref}}{4}\right)$$

$$= -2.54 + 30m < 0$$

$$\downarrow$$

$$b_1 = 0$$

- i = 2

$$V_2 = -2.51V < 0$$

$$\downarrow$$

$$V_2 \rightarrow 2\left(V_2 + \frac{V_{ref}}{4}\right)$$

$$= -0.02 + 30m > 0$$

$$\downarrow$$

$$b_2 = 1$$

- i = 3

$$V_3 = 0.01V > 0$$

$$\downarrow$$

$$V_3 \rightarrow 2\left(V_3 - \frac{V_{ref}}{4}\right)$$

$$= -4.98 + 30m < 0$$

$$\downarrow$$

$$b_3 = 0$$

- i = 4

$$V_4 = -4.95V < 0$$

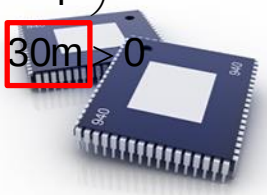
$$\downarrow$$

$$V_4 \rightarrow 2\left(V_4 + \frac{V_{ref}}{4}\right)$$

$$= -4.96 + 30m > 0$$

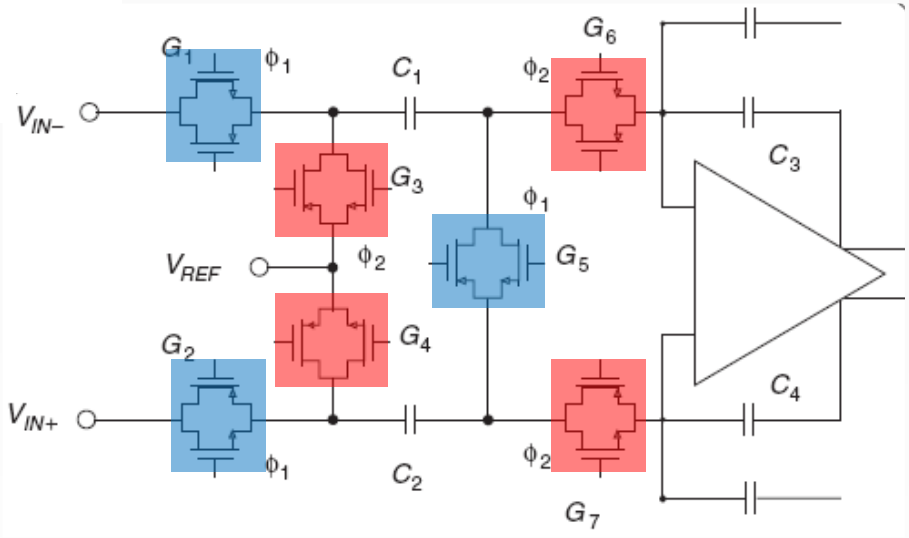
$$\downarrow$$

$$b_4 = 0$$



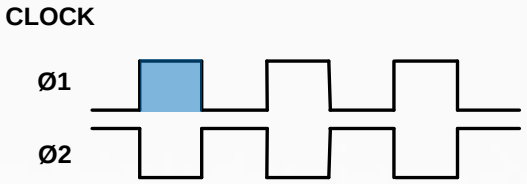
Algorithmic (or cyclic) A/D converters

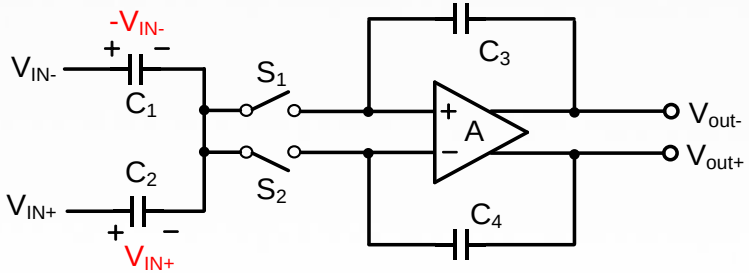
Multiply-by-two gain circuitry



Multiply-by-two gain circuitry

① $Ø_1$(rising edge) : G1, G2, G5 turn on ⇒ V_{IN} sampling



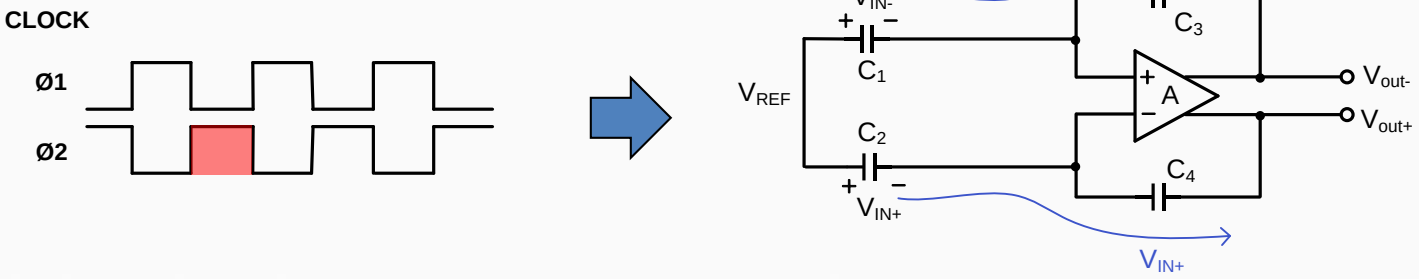


- **Operation**
  - **Ø1 : G1, G2, G5**
  - **Ø2 : G3, G4, G6, G7**

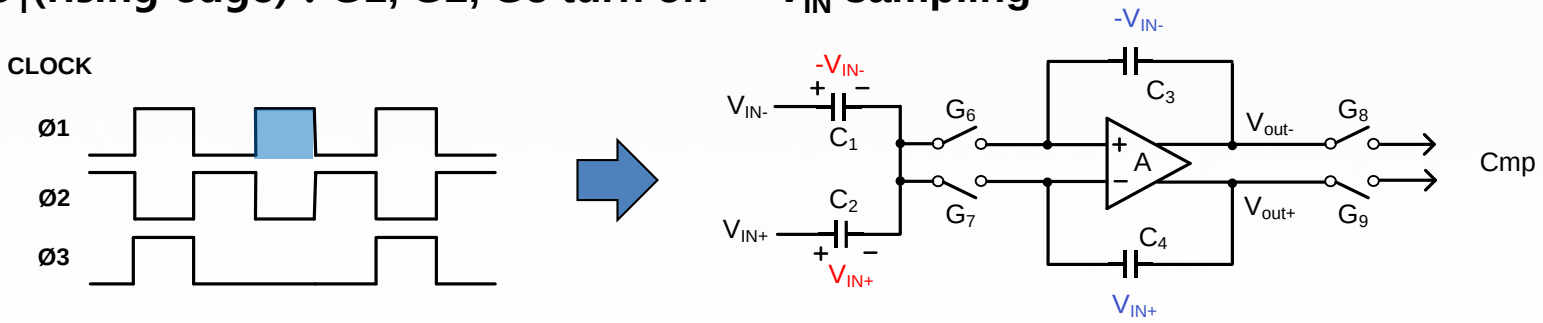
Algorithmic (or cyclic) A/D converters

Multiply-by-two gain circuitry

② $Ø_2$(falling edge) : G3, G4, G6, G7 turn on



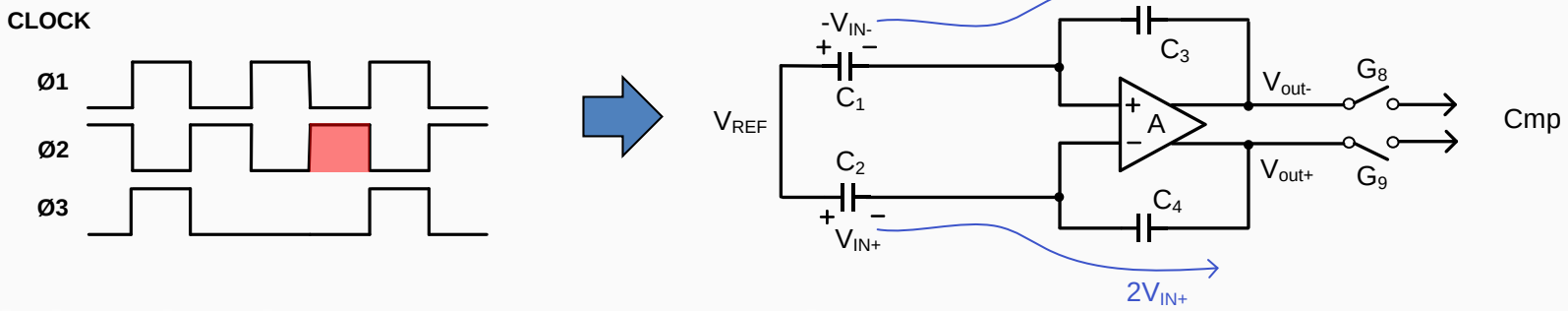
③ $Ø_1$(rising edge) : G1, G2, G5 turn on ⇒ V_{IN} sampling



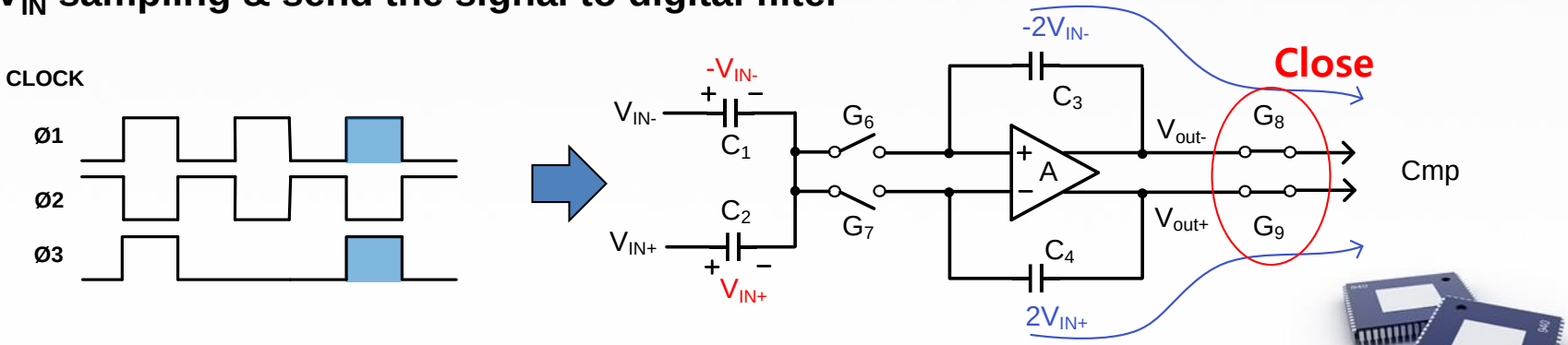
Algorithmic (or cyclic) A/D converters

Multiply-by-two gain circuitry

④ $Ø_2$(falling edge) : G3, G4, G6, G7 turn on

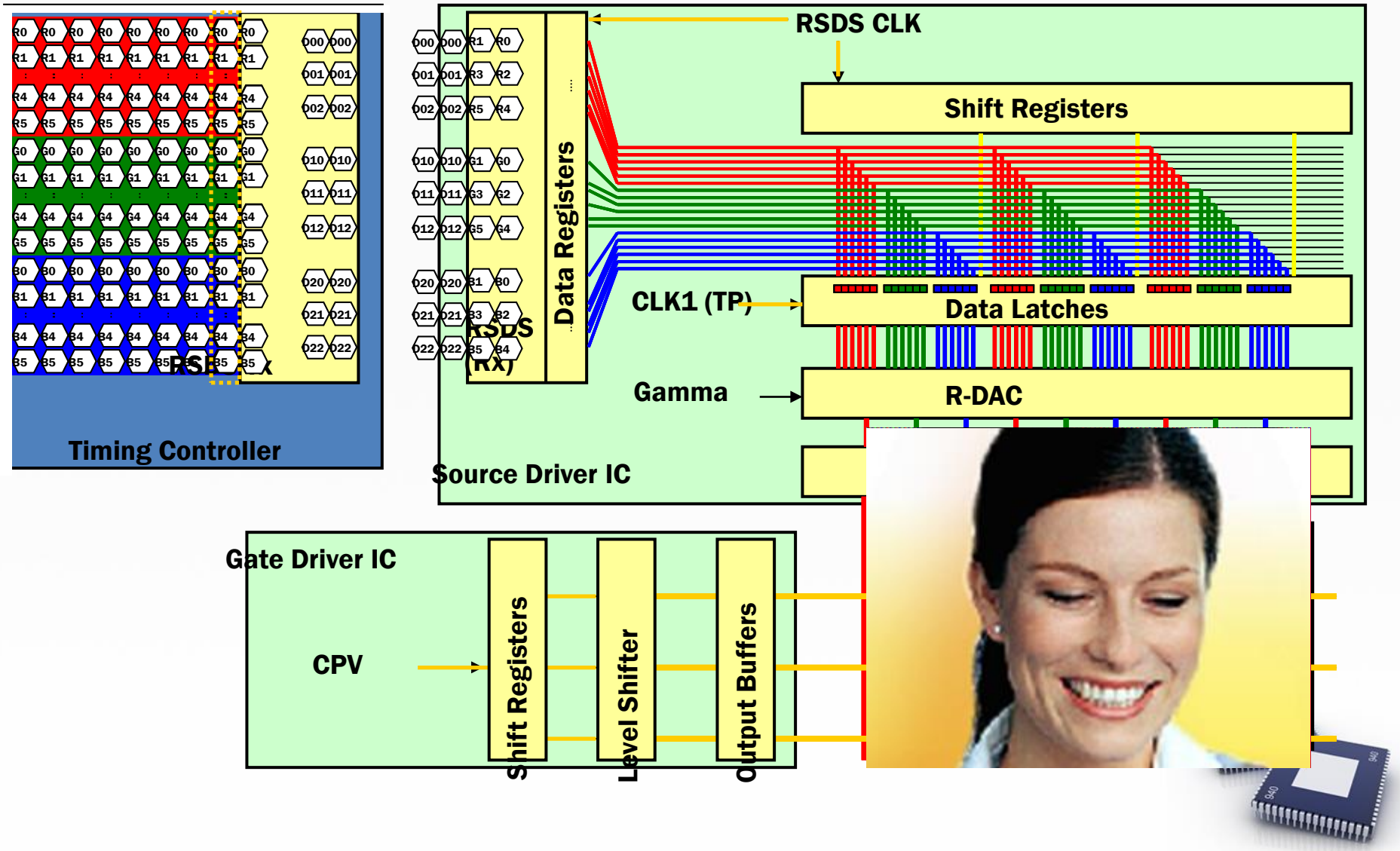


⑤ $Ø_2$(rising edge) : G1, G2, G5, G8, G9 turn on
⇒ V_{IN} sampling & send the signal to digital filter



17. Nyquist-rate A/D converter

Operation of LCD



Basic Operation

SAR & Algorithmic converter

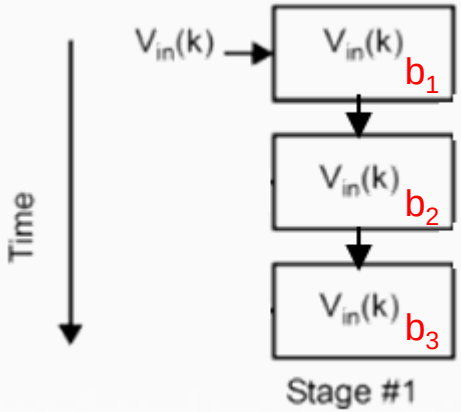


Fig. The signal flow in SAR & algorithmic converter.

Pipelined converter

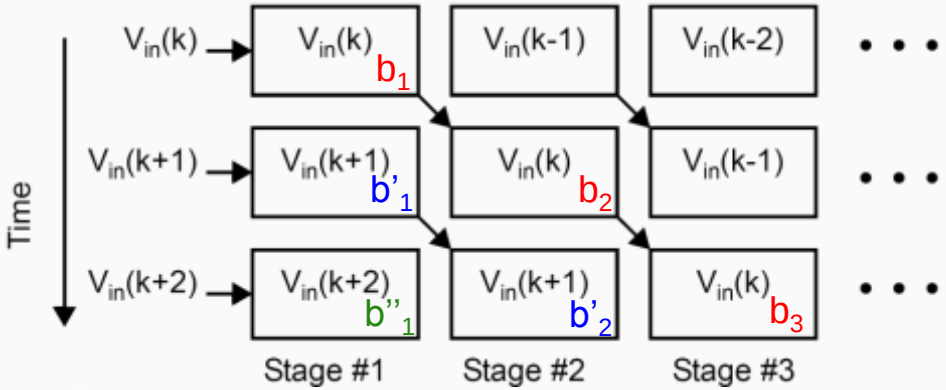


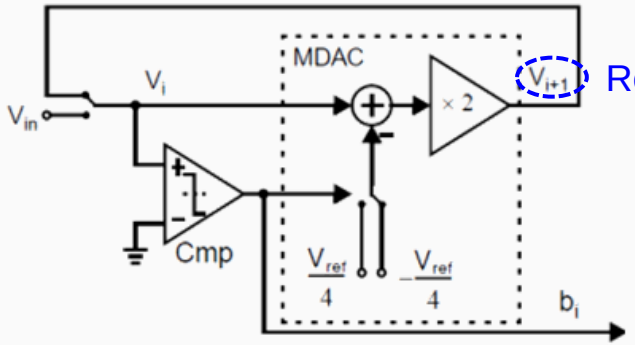
Fig. 17.17 The signal flow in a pipelined A/D converter.

- **Area & power consumption ↓**
- **Requires N step for N-bit converter**

- **Higher throughput**
- **Need initial N step latency**
  Area & power consumption ↑

Basic Operation

Algorithmic converter

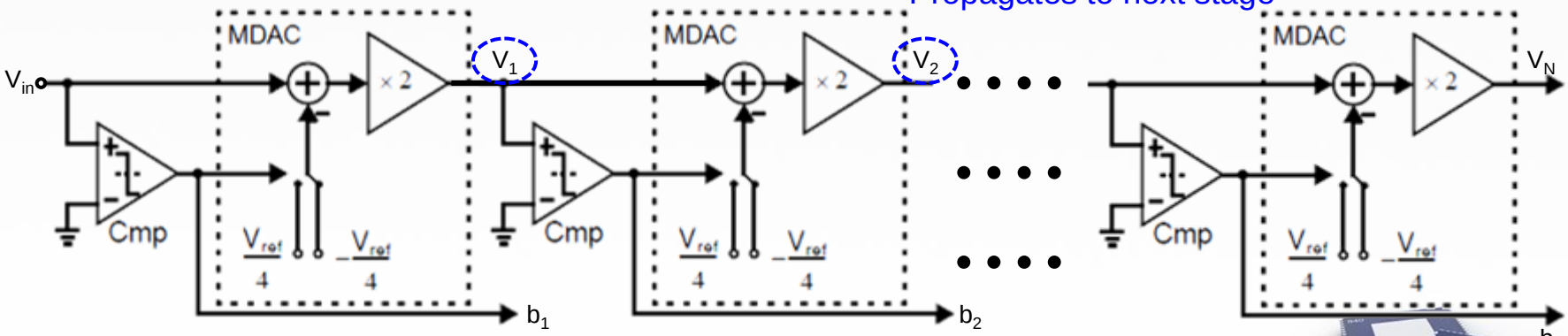


Returns to input of the converter

→ ***Iteration of single analog circuit***

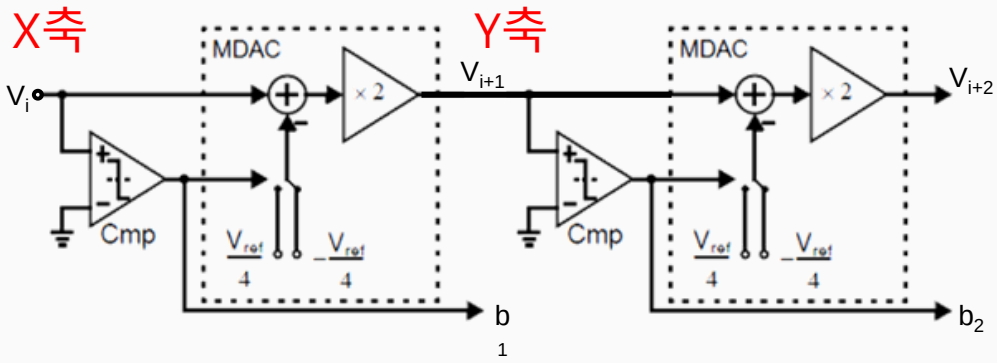
Pipelined converter

Propagates to next stage



→ ***Iteration of N-stage analog circuits***

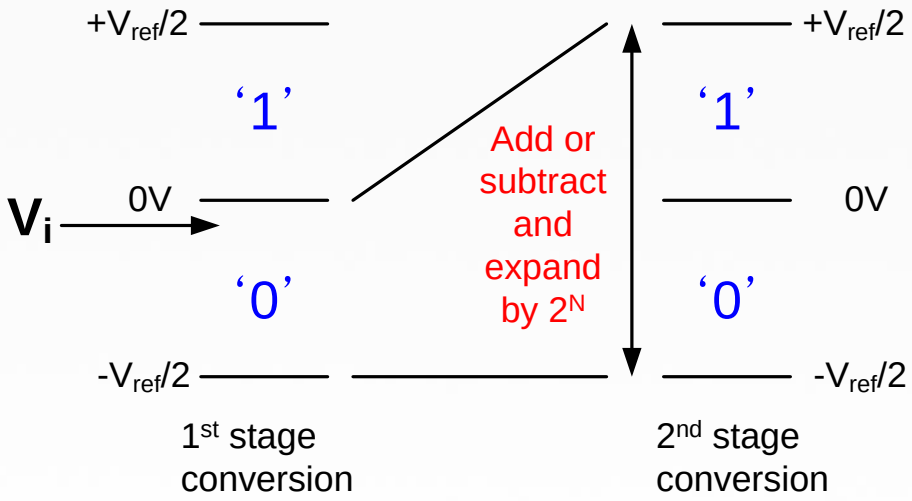
One-Bit-Per-Stage Pipelined ADC

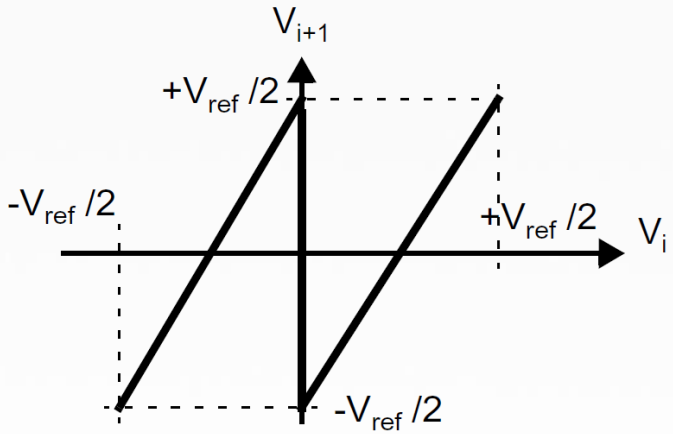


$$V_{i+1} = 2[V_i + (b_i - 0.5)V_{ref} / 2] \quad (17.39)$$

Residue signal

$$V_{i+1} = 2V_i \pm V_{ref} / 2$$





Each stages consists of same circuits in pipeline ADC

One-Bit-Per-Stage Pipelined ADC

In order to realign the bits in time

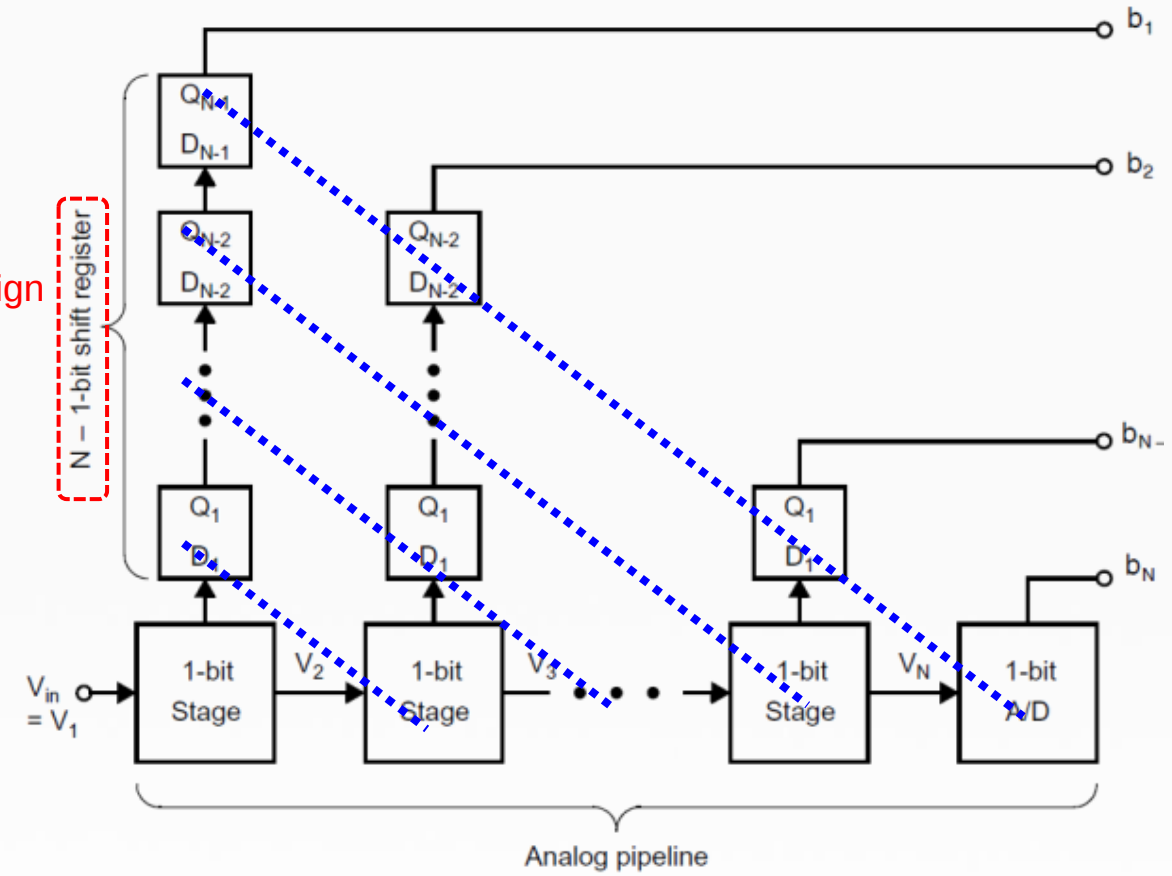
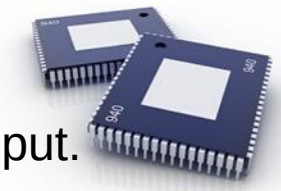


Fig. 17.19 A one-bit-per-stage pipelined A/D converter [Martin, 1981].

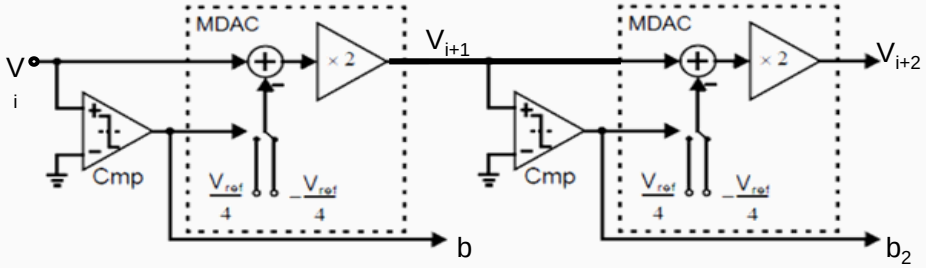
$$\hat{V}_{in} = V_{ref} \sum_{i=1}^{N} (b_i - 0.5)2^{-i} \qquad (17.40)$$

- Residue voltage : N-bit quantized estimate of the original input.



Example 3

Consider the operation of a 3-bit, one bit per stage pipelined converter with V_{ref} = 1V(0V±0.5V). Find final output digital code, all the residue voltages, V_i, and the for a sampled input voltage of V_{in} = 240mV.



$$V_1 = V_{in} = 240mV \qquad V_{i+1} = 2[V_i - (b_i - 0.5)V_{ref} / 2] \qquad (17.39)$$

① $b_1 = 1$ $\quad V_2 = 2(V_1 - V_{ref} / 4) = -20mV$

② $b_2 = 0$ $\quad V_3 = 2(V_2 + V_{ref} / 4) = 460mV$

③ $b_3 = 1$ ➢ Final output code $b_1 b_2 b_3 = 101$

➢ All the residue voltage :

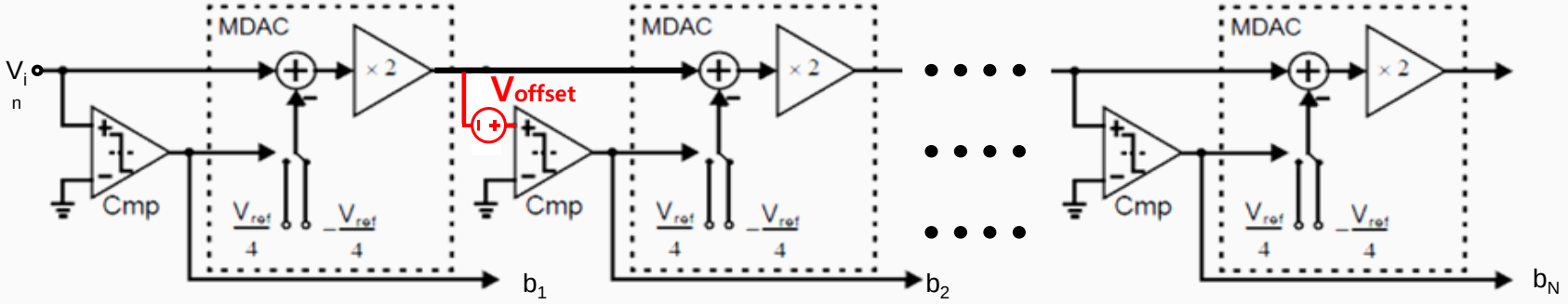
$$\hat{V}_{in} = V_{ref} \sum_{i=1}^{N} (b_i - 0.5)2^{-i} \qquad (17.40)$$

$$\hat{V}_{in} = 1 \times \left[(1-0.5)2^{-1} \times (0-0.5)2^{-2} \times (1-0.5)2^{-3} \right]$$

$$\hat{V}_{in} = 187.5mV$$

Example 4

What will happen if the comparator in the second stage has an offset of 30 mV ?



$V_1 = V_{in} = 240mV$ $\qquad V_{i+1} = 2[V_i - (b_i - 0.5)V_{ref} / 2]$ (17.39)

① $b_1 = 1$ $\qquad V_2 = 2(V_1 - V_{ref} / 4) = -20mV$ (+ 30mV)

② $b_2 = 1$ $\qquad V_3 = 2(V_2 - V_{ref} / 4) = -540mV$

③ $b_3 = 0$

- Final output code $b_1 b_2 b_3 = 110$

$$\hat{V}_{in} = V_{ref} \sum_{i=1}^{N} (b_i - 0.5)2^{-i} \quad (17.40)$$

$\hat{V}_{in} = 375mV$ ⇒ 오프셋에 의한 입력전압과의 오차: **135 mV,**
(오프셋이 없을 경우: **52.5 mV)**