LECTURE 5

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6. Basic Opamp Design and Compensation

6.1 Two-Stage CMOS Opamp

6.2 Opamp Compensation

6.3 Advanced Current Mirrors

6.4 Folded-Cascode Opamp

Two-Stage CMOS Opamp

- The two-stage circuit architecture has been the most popular approach

- **High gain, Large swing**

Compensation capacitor for stability

Differential-input
single-ended output stage

Output buffer for gain

V_{in} $-A_1$ C_{cmp} $-A_2$ 1 V_{out}

Differential
input stage
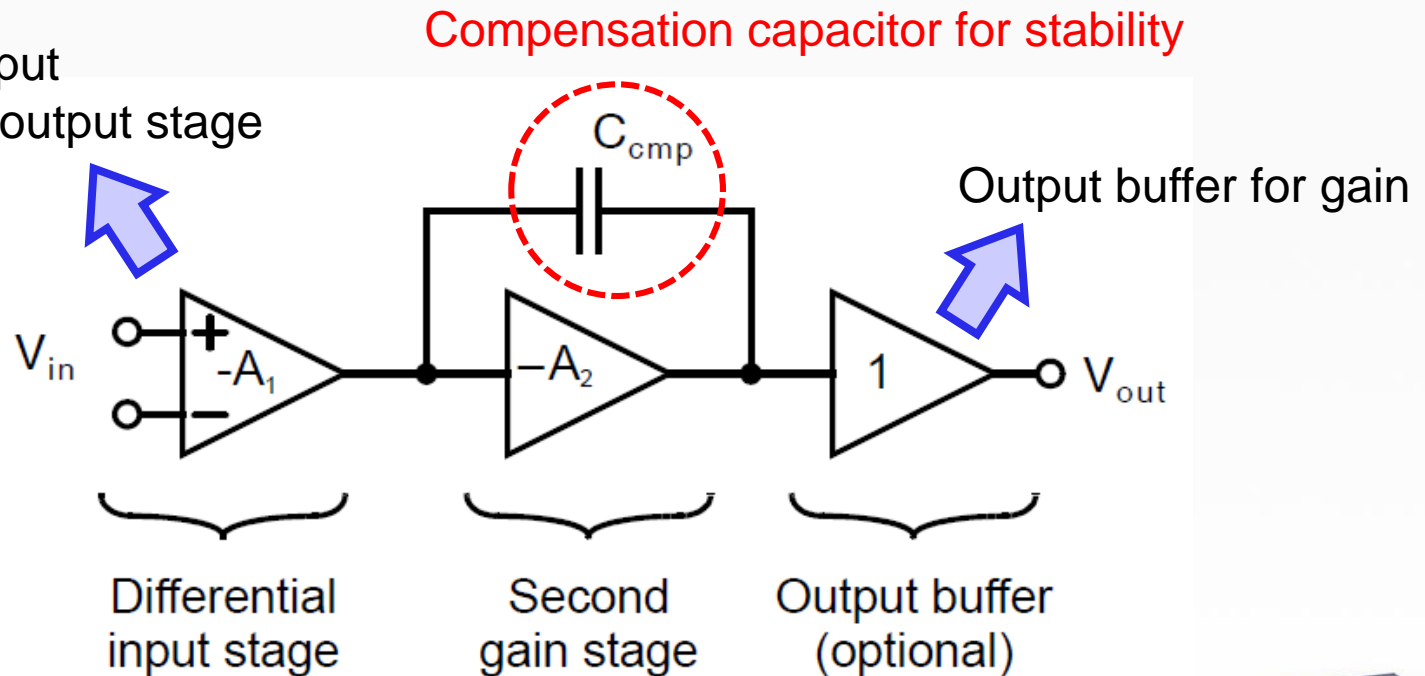
Second
gain stage

Output buffer
(optional)

Fig. 6.2 A block diagram of a two-stage opamp.

1

Opamp Gain

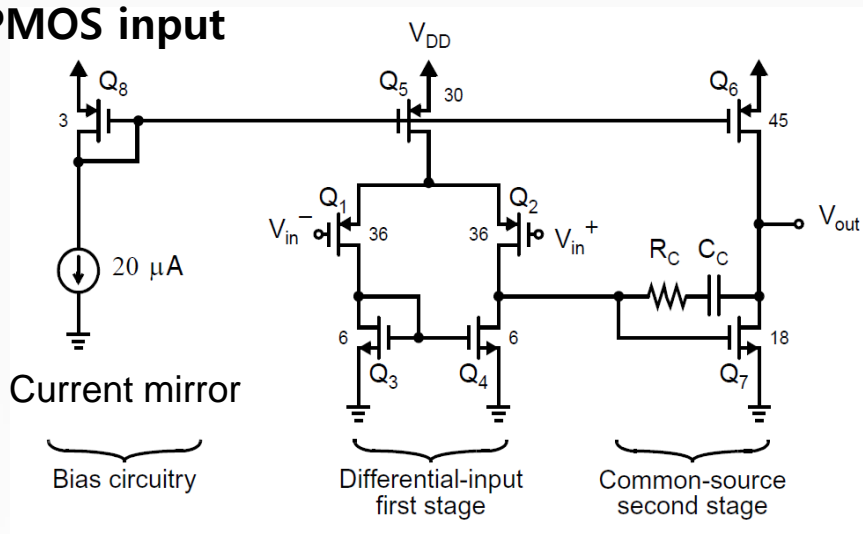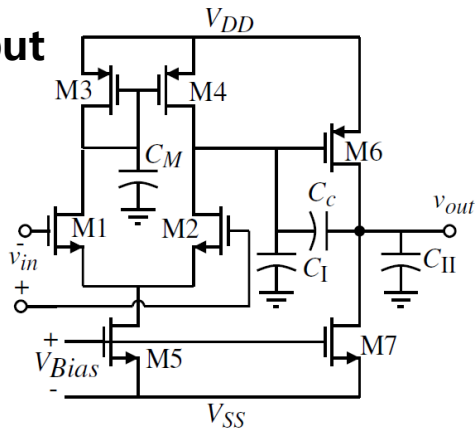- Gain is one of the most critical parameters of an opamp

PMOS input

Fig. 6.3 A CMOS two-stage amplifier.

NMOS input

$$A_{v1} = -g_{m1}\left(r_{ds2} \| r_{ds4}\right) \qquad (6.1)$$

$$g_{m1} = \sqrt{2\mu_p C_{OX}\left(\frac{W}{L}\right)_1 I_{D1}}$$

$$= \sqrt{2\mu_p C_{OX}\left(\frac{W}{L}\right)_1 \frac{I_{bias}}{2}} \qquad (6.2)$$

$$A_{v2} = -g_{m7}\left(r_{ds6} \| r_{ds7}\right) \qquad (6.3)$$

2

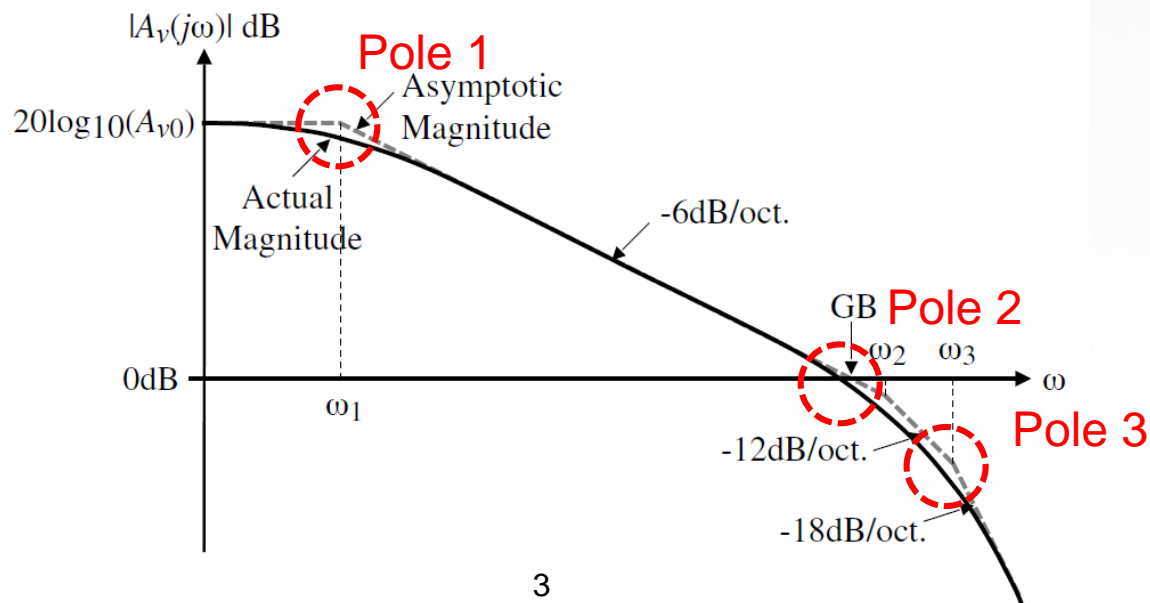# Frequency Response

- **Linear and Dynamic Characteristics of the Opamp**

  Differential and common-mode frequency response :

  $$V_{out}(s) = A_v(s)[V_1(s) - V_2(s)] \pm A_c(s)\left(\frac{V_1(s)+V_2(s)}{2}\right)$$

  Differential-frequency response :

  $$A_v(s) = \frac{A_{v0}}{\left(1+\dfrac{s}{\omega_1}\right)\left(1+\dfrac{s}{\omega_2}\right)\left(1+\dfrac{s}{\omega_3}\right)\cdots}$$

3

Slew Rate

- The slew rate : opamp의 아웃풋 전압이 바뀌는 최대의 기울기

$$SR \equiv \left.\frac{dv_{out}}{dt}\right|_{max} = \frac{I_{C_C}\big|_{max}}{C_C} = \frac{I_{D5}}{C_C}$$
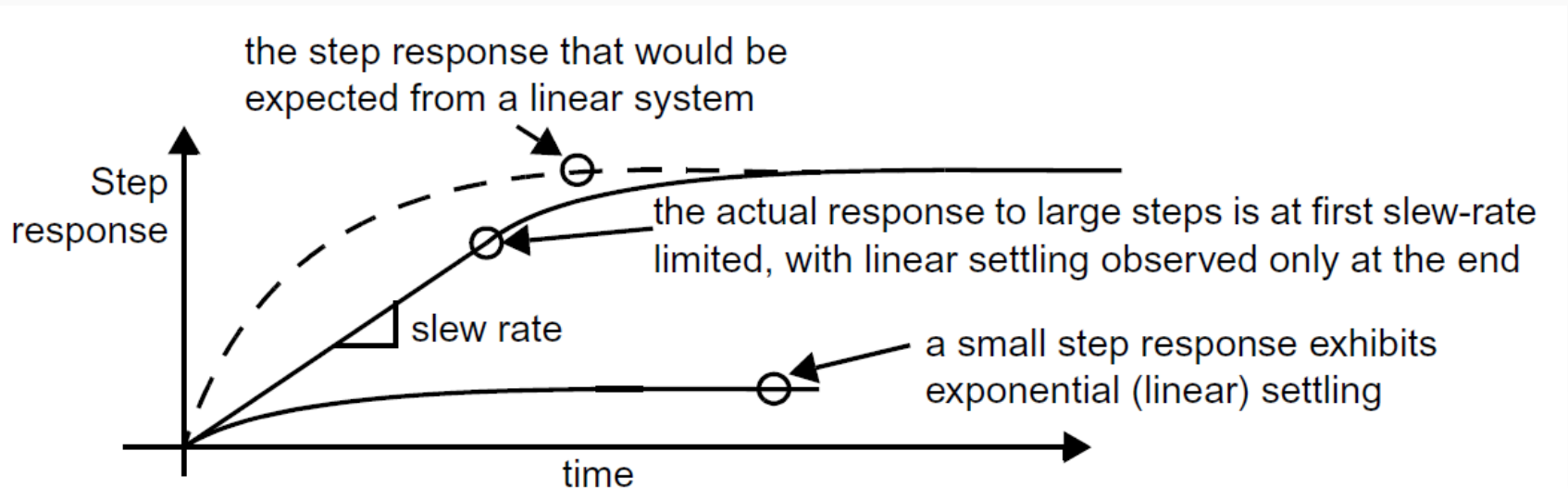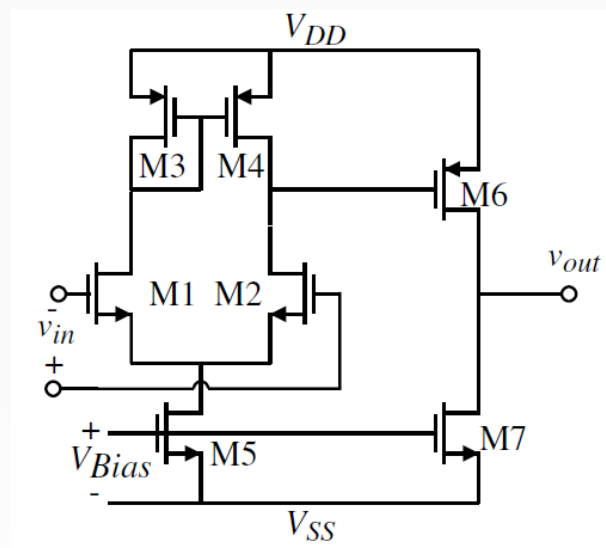
(6.25)

Fig. 6.6 An illustration of the effect of slew-rate limiting in opamps.
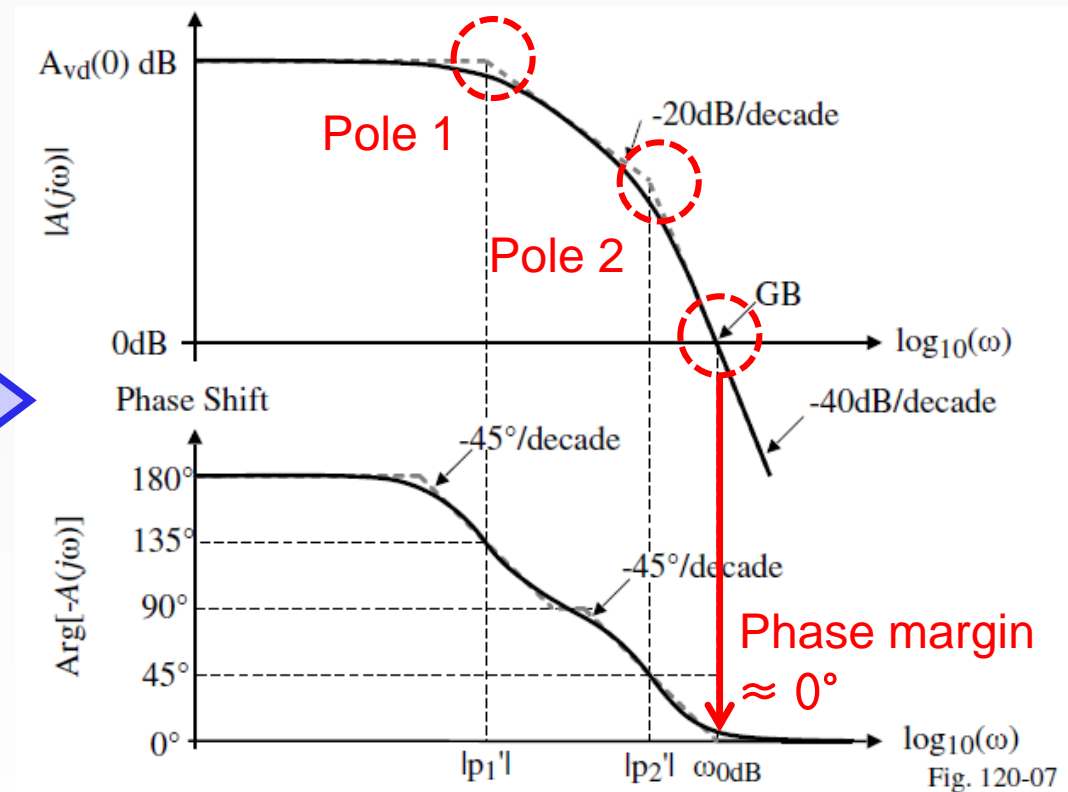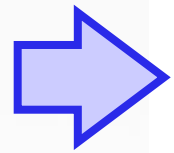
Design procedure for compensation

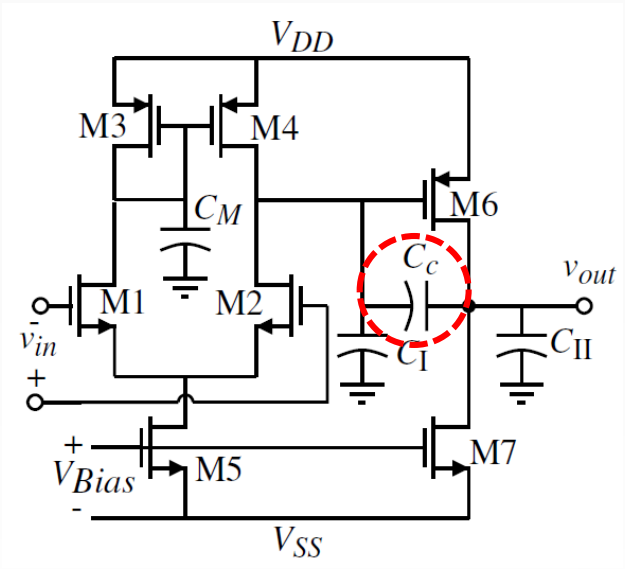- **Uncompensated** frequency response of two-stage opamps

Uncompensated two-stage opamp

Phase margin is almost 0°!

Design procedure for compensation

- **Miller compensation** of the two-stage opamps

C_C = **Miller capacitor**
C_M = First-stage mirror capacitor
C_I = output capacitance of first-stage
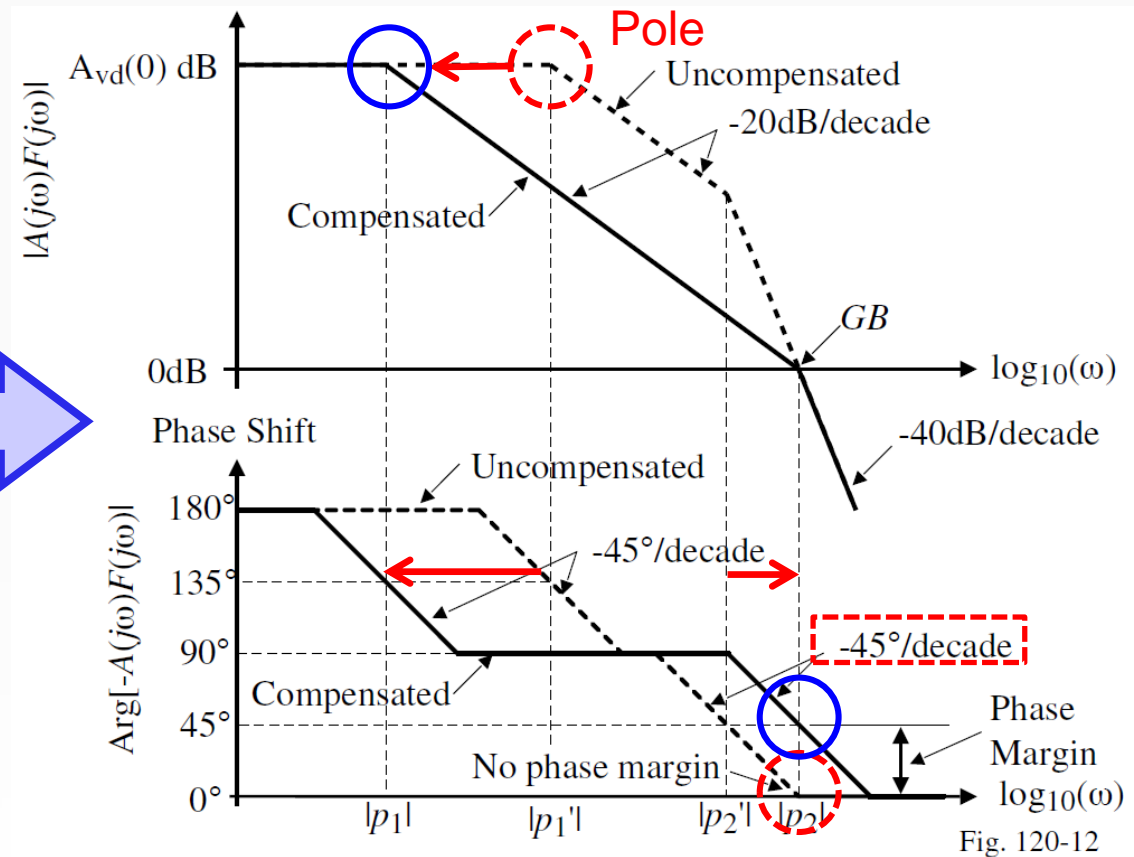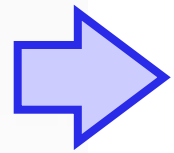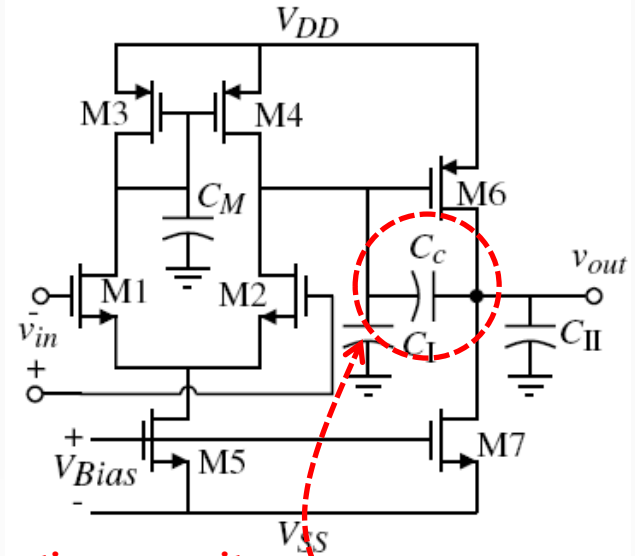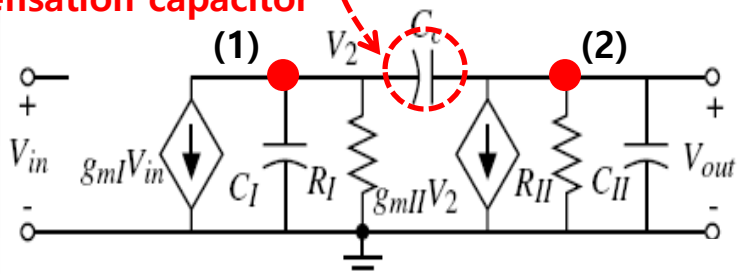C_{II} = output capacitance of second-stage

A bode plot of open-loop gain illustrating dominant-pole and lead compensation.

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Frequency characteristic

Compensation capacitor

Miller capacitance applied to the two-stage op amp

$$g_{mI} = g_{m1} = g_{m2},\ R_I = r_{02} \parallel r_{04}$$

$$g_{mII} = g_{m6},\ R_{II} = r_{06} \parallel r_{07}$$

− KCL

(1) $\ 0 = g_{mI} V_{in} + \left(sC_I + \dfrac{1}{R_I} \right) V_2 + \left(V_2 - V_{out} \right) \cdot sC_c$

(2) $\ 0 = g_{mII} V_2 + \left(V_{out} - V_2 \right) \cdot sC_c + V_{out} \left(\dfrac{1}{R_{II}} + sC_{II} \right)$

$$V_2 = \dfrac{sC_c + \dfrac{1}{R_{II}} + sC_2}{\left(sC_c - g_{mII} \right)} \cdot V_{out}$$

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Frequency characteristic

A_o

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{mI}g_{mII}R_{I}R_{II}\left[1-s\left(C_c/g_{mII}\right)\right]}{1+s\underbrace{\left[R_{I}\left(C_{I}+C_c\right)+R_{II}\left(C_{II}+C_c\right)+g_{mII}R_{I}R_{II}C_c\right]}_{-1/p_1}+s^2\underbrace{R_{I}R_{II}\left[C_{I}C_{II}+C_cC_{I}+C_cC_{II}\right]}_{1/p_1p_2}}$$

– In general,

$$D(s) = \left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right) = 1-s\left(\frac{1}{p_1}+\frac{1}{p_2}\right)+\frac{s^2}{p_1p_2} \rightarrow D(s) \approx 1-\frac{s}{p_1}+\frac{s^2}{p_1p_2}, \text{ if } |p_2| \gg |p_1|$$

$$p_1 = \frac{-1}{\left[R_{I}\left(C_{I}+C_c\right)+R_{II}\left(C_{II}+C_c\right)+g_{mII}R_{I}R_{II}C_c\right]} \approx \frac{-1}{g_{mII}R_{I}R_{II}C_c}$$

$$p_2 \cong \frac{-g_{mII}C_c}{C_{I}C_{II}+C_{II}C_c+C_{I}C_c} \approx \frac{-g_{mII}}{C_{II}}$$

$$\left(\because C_{II} > C_c > C_{I}\right)$$

$$z = \frac{g_{mII}}{C_{II}}$$

➢ **Right-half plane zero**
Magnitude ↑, Phase ↓
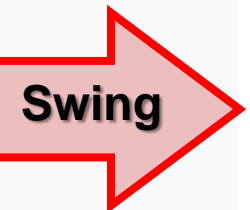Unstable!!

Wide-Swing Current Mirrors

Conventional

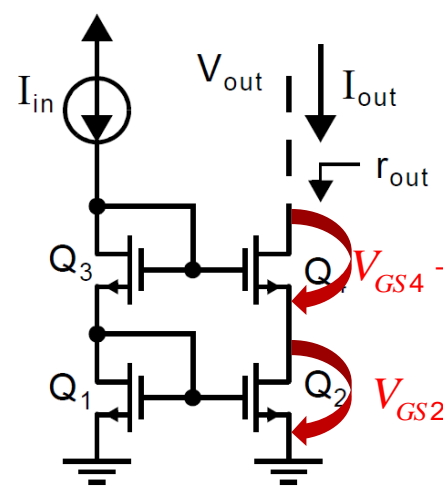**Low-voltage current mirror**
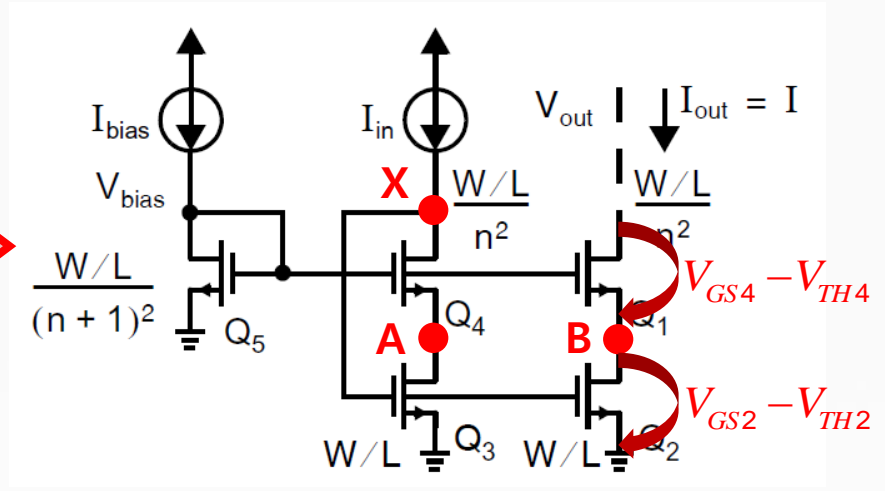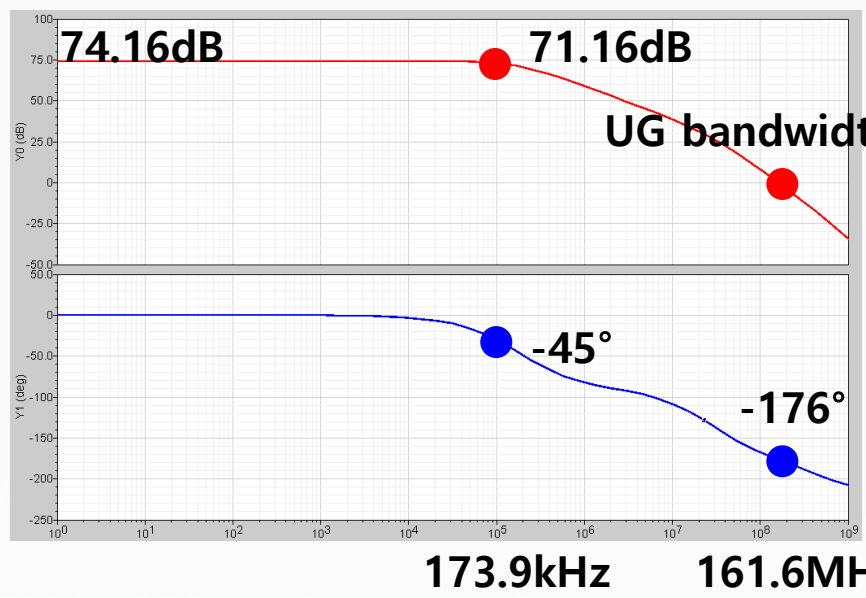

Fig. 3.14 A cascode current mirror

Fig. 6.12 Wide-swing cascode current mirror

🙂 **Low voltage drop**

🙁 **Increase the power dissipation**

Simulation result

Without compensation capacitor

74.16dB   **71.16dB**

UG bandwidth

-45°

-176°

173.9kHz   **161.6MHz**

With compensation capacitor

74.16dB   **71.16dB**

UG bandwidth

-45°

-130°

14.68kHz   **64.66MHz**
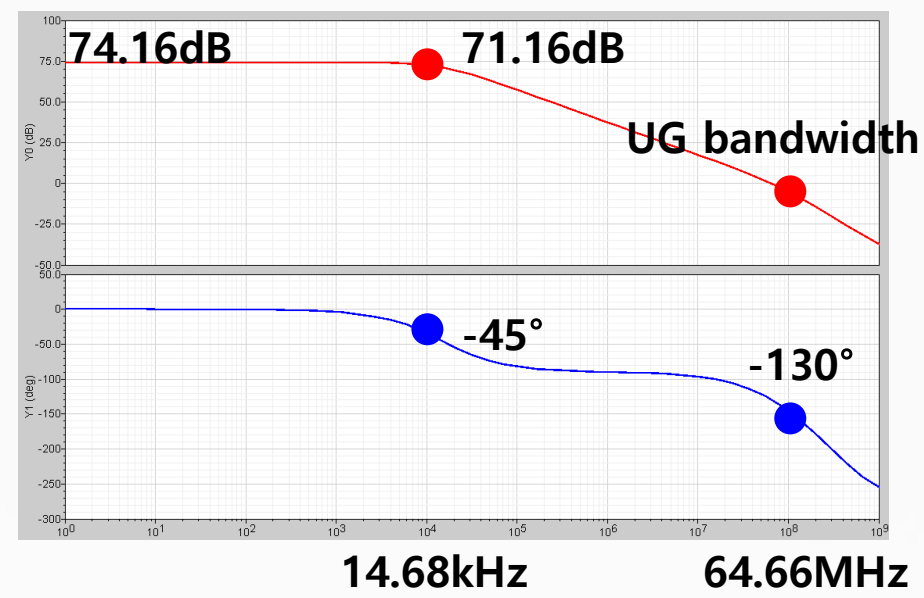
Compensation capacitor

$$p_1 = \frac{-1}{R_I \cdot C_I}$$

$$R_I = r_{ds2} \parallel r_{ds4}$$

$$R_{II} = r_{ds6} \parallel r_{ds7}$$

$$C_I = C_{gs6} + C_{bd2} + C_{bd4}$$

$$C_{II} \approx C_L$$

1. **Dominant pole ↓**
2. **Phase margin ↑** 🙂
3. **Unity-gain bandwidth ↓** 😕
4. **Gain is same**

$$p_1 \approx \frac{-1}{g_{mII} R_I R_{II} C_C}$$

$$R_I = r_{ds2} \parallel r_{ds4}$$

$$R_{II} = r_{ds6} \parallel r_{ds7}$$

$$C_I \approx C_{gs6} + C_{bd2} + C_{bd4} + A_{v2} \cdot C_C$$

$$C_{II} \approx C_L$$