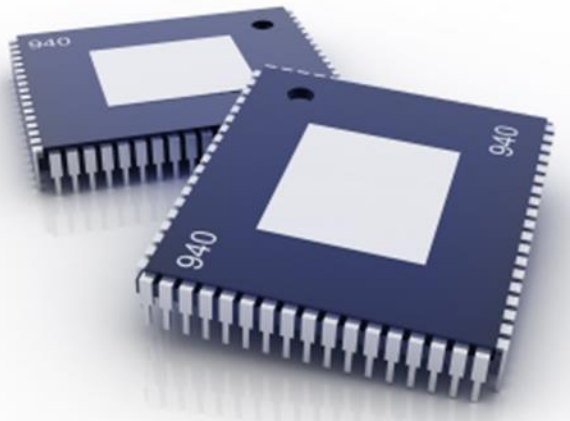

LECTURE 11

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15. Data converter fundamentals

Ideal D/A converter

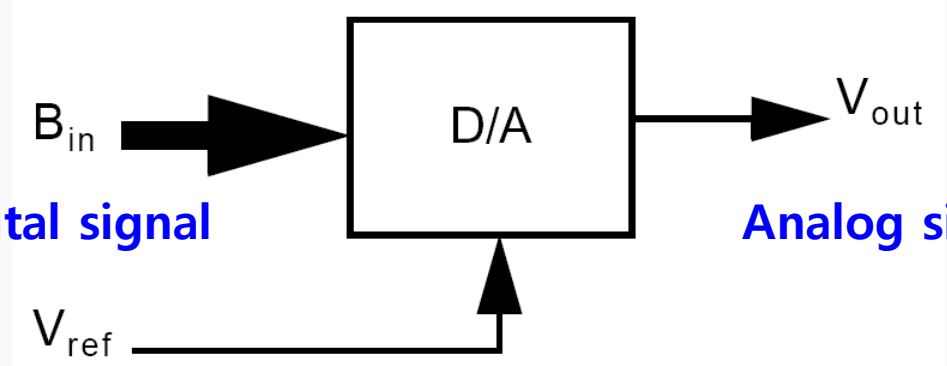


Fig. 15.1 A block diagram representing a D/A converter

- B_{in} : N-bit digital signal

$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N} \quad (15.1)$$

- b_i : 1 or 0, binary digit
  - b_1 : MSB
  - b_N : LSB

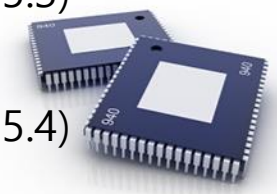
- V_{out} : analog signal

$$V_{out} = V_{ref}\left(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}\right)$$
$$= V_{ref} B_{in} \quad (15.2)$$

- V_{LSB} : LSB (least significant bit)

$$V_{LSB} \equiv \frac{V_{ref}}{2^N} \quad (15.3)$$

$$1LSB = \frac{1}{2^N} \quad (15.4)$$



Example 1

What is the V_{out} and V_{LSB} when B_{in}=10110100?

Assume that V_{ref} = 5V, 8bit DAC

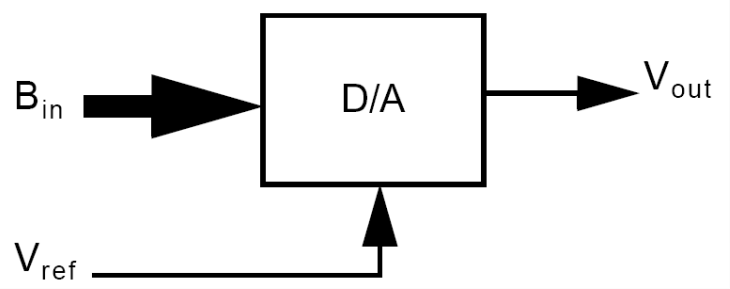


Fig. 15.1 A block diagram representing a D/A converter

Bin = 10110100

$$B_{in} = 2^{-1} + 2^{-3} + 2^{-4} + 2^{-6} \qquad (15.5)$$

$$V_{out} = V_{ref} B_{in} = 5 \cdot 0.7031 \approx 3.516V \qquad (15.6)$$

$$V_{LSB} = \frac{V_{ref}}{2^N} = \frac{5}{256} = 19.5mV \qquad (15.7)$$

Ideal A/D converter

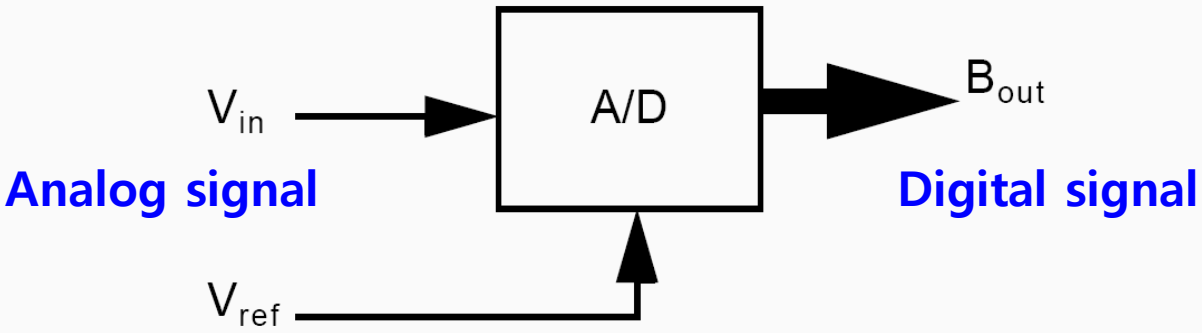


Fig. 15.3 A block diagram representing an A/D converter

- V_{in} : analog signal

$$V_{ref}\left(b_1 2^{-1}+b_2 2^{-2}+\ldots+b_N 2^{-N}\right) = V_{in} \pm V_x$$

$$-\frac{1}{2}V_{LSB} \le V_x \le \frac{1}{2}V_{LSB} \qquad (15.8)$$

$$-\frac{1}{2}V_{LSB} \le V_x \le \frac{1}{2}V_{LSB}$$

⇨ **Quantization error(V_{LSB})**

Range of input values that produce the same digital output word

Input-output transfer curve

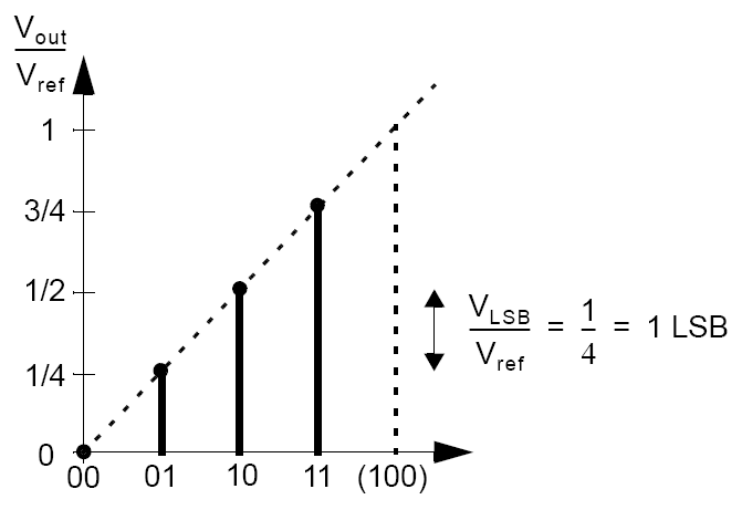


Fig. 15.2 Input-output transfer curve for an ideal 2-bit D/A converter

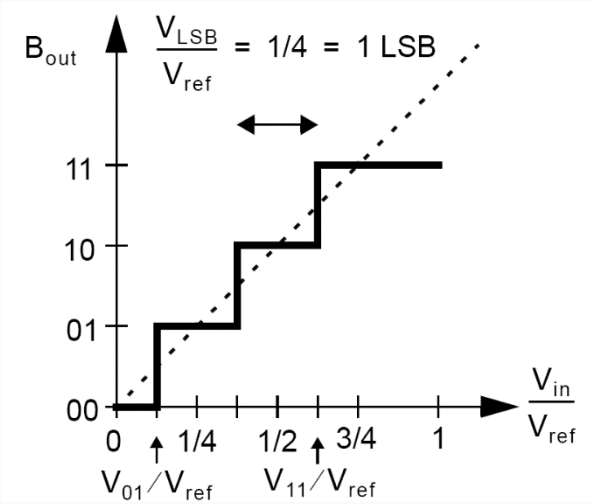


Fig. 15.4 Input-output transfer curve for a 2-bit A/D converter

D-A converter

- Not quantization error
- Maximum value of Vout $\neq V_{ref}$

$$V_{out,\mathbf{max}} = V_{ref}\left(1-2^{N}\right)$$
$$= V_{ref} - V_{LSB}$$

A-D converter

- quantization error ($1V_{LSB}$)
- Quantizer Overload

$$Quantization\ error > 1 \cdot V_{LSB}$$

Quantization noise

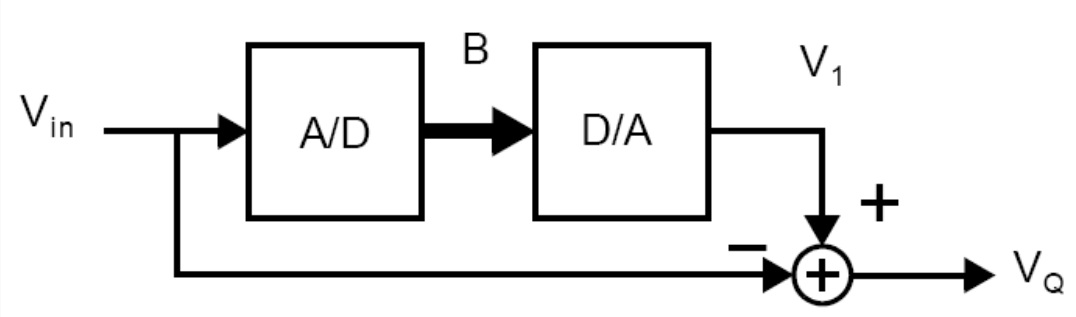
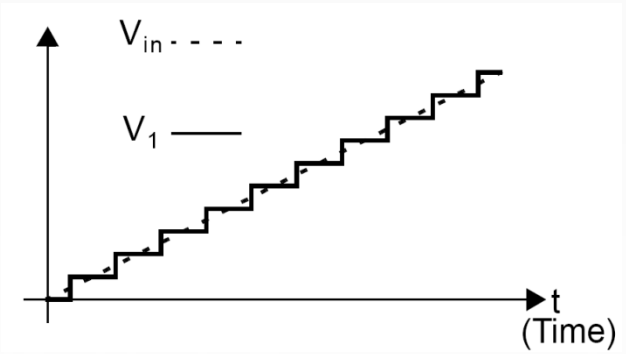


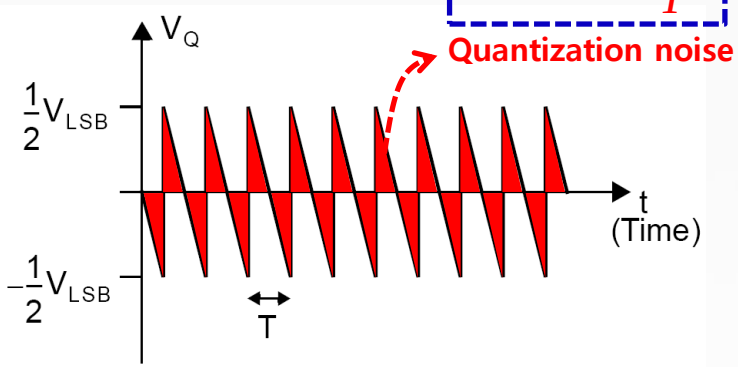
Fig. 15.5 A circuit to investigate quantization noise behavior

$$V_Q = V_{LSB} \cdot \frac{-t}{T}$$

Quantization noise



(a)



(b)

Fig. 15.6 Applying a ramp signal to the circuit in Fig. 15.5

$$V_Q = V_1 - V_{in} \quad (15.9)$$

$$V_1 = V_{in} + V_Q \quad (15.10)$$

SQNR & SNR

Signal-to-quantization noise ratio (SQNR)

$$SQNR = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) \qquad (15.15)$$

$$V_{Q(rms)} = \left[\frac{1}{T}\int_{-T/2}^{T/2} V_Q^2\, dt\right]^{1/2} \Leftarrow \left(V_Q = V_{LSB}\cdot\frac{-t}{T}\right)$$

$$= \left[\frac{1}{T}\int_{-T/2}^{T/2} (V_{LSB})^2\left(\frac{-t}{T}\right)^2 dt\right]^{1/2}$$

$$= \left[\frac{V_{LSB}^2}{T^3}\left(\frac{t^3}{3}\Big|_{-T/2}^{T/2}\right)\right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}} \qquad (15.11)$$

Assume $V_{in} = Sin\ wave$

$$V_{in(rms)} = \left[\frac{1}{T}\int_{-T/2}^{T/2}\left(\frac{V_{ref}}{2}\sin wt\right)^2 dt\right]^{1/2}$$

$$= \left[\frac{1}{T}\frac{V_{ref}^2}{8}\Big|_{-T/2}^{T/2} - \frac{1}{4w}\sin 2wt\Big|_{-T/2}^{T/2}\right]^{1/2}$$

$$= \frac{V_{ref}}{2\sqrt{2}}$$

$$SNQR = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{ref}\ /\ 2\sqrt{2}}{V_{LSB}\ /\ \sqrt{12}}\right)$$

$$= 20\log\left(\sqrt{\frac{3}{2}}2^N\right) = 6.02N + 1.76\ dB \qquad (15.16)$$

SQNR = Best possible SNR(signal to noise ratio)

Example 2

Find the $V_{Q(rms)}$, SQNR for full-scale, half-scale sine wave. Assume that 10-bit A/D converter, V_{ref} = 2V.

V_Q(rms) using (15.3) and (15.11),

$$V_{LSB} \equiv \frac{V_{ref}}{2^N} = \frac{2}{2^{10}} = 1.9531mV \qquad (15.17) \qquad V_{Q(rms)} = \frac{V_{LSB}}{\sqrt{12}} = \frac{1.9531mV}{\sqrt{12}} = 0.564mV$$

SQNR for full-scale sine wave Using (15.16),

$$SQNR = 6.02N + 1.76\ dB = 6.02 \cdot 10 + 1.76 = 61.96dB$$

SQNR for half-scale sine wave Using (15.16),

RMS of half-scale is half of full scale,

$$SQNR = 20\log\left(\frac{\frac{V_{in(rms)}}{2}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) - 20\log(2)$$

$$= SQNR_{full-scale} - 6.02 = 61.96 - 6.02 = 55.94dB$$

Example 2 (Cont'd)

Find the number of bits when SQNR = 80dB for full-scale, half-scale sine wave. Assume that 10-bit A/D converter, V_{ref} = 2V.

SQNR using (15.16)

$$SQNR = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{ref}/2\sqrt{2}}{V_{LSB}/\sqrt{12}}\right) \qquad (15.16)$$

$$= 20\log\left(2^N\right) = 6.02N + 1.76\ dB$$

# of bits for full-scale sine wave Using (15.16),

$$SQNR = 6.02N + 1.76\ dB = 80dB$$

$$N \Rightarrow 13 \quad \Rightarrow \quad 2^{13} = 8192$$

# of bits for half-scale sine wave Using (15.16),

$$SQNR = SQNR_{full-scale} - 6.02 = 80dB$$

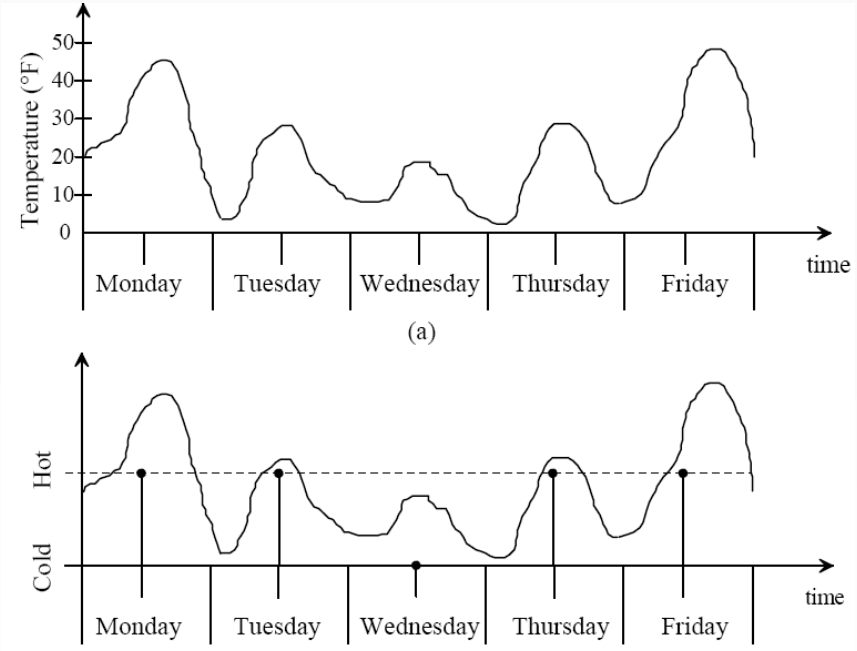
$$SQNR_{full-scale} = 86.02dB, \quad N \Rightarrow 14 \quad \Rightarrow \quad 2^{14} = 16384$$

Performance limitation

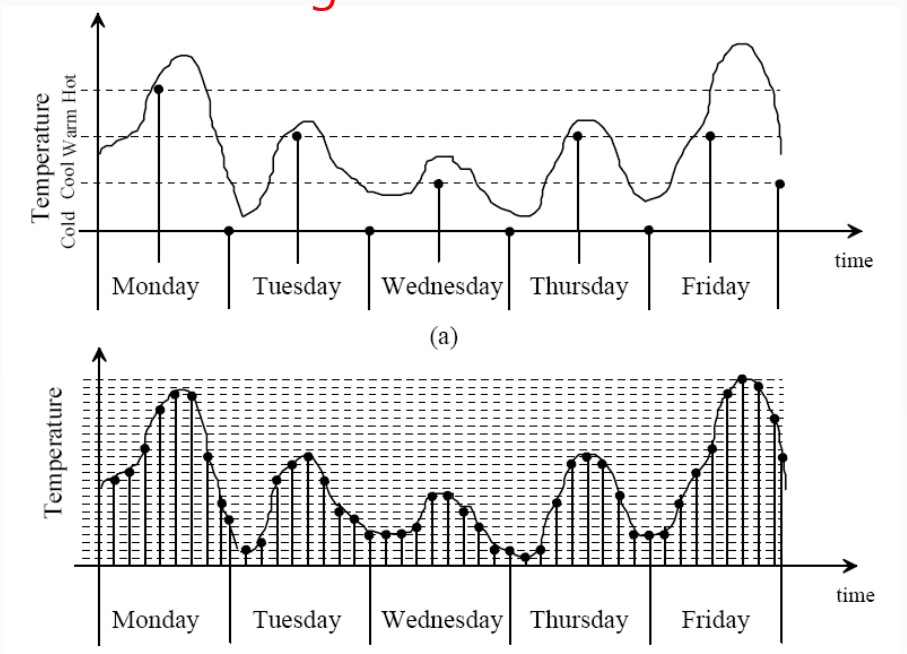
- High resolution
- Offset error
- Gain error
- INL & DNL
- Monotonic

Resolution

Low resolution

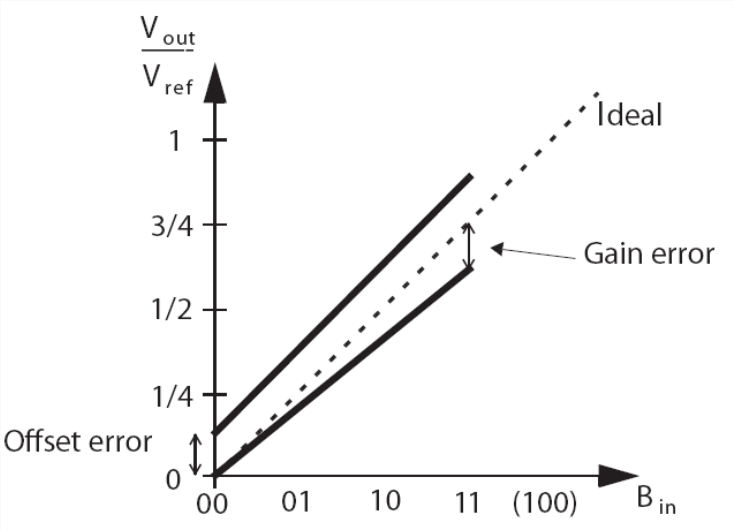


High resolution



Accuracy of digitalized signal: # of samples taken, resolution (# of quantization levels)

Offset and Gain error



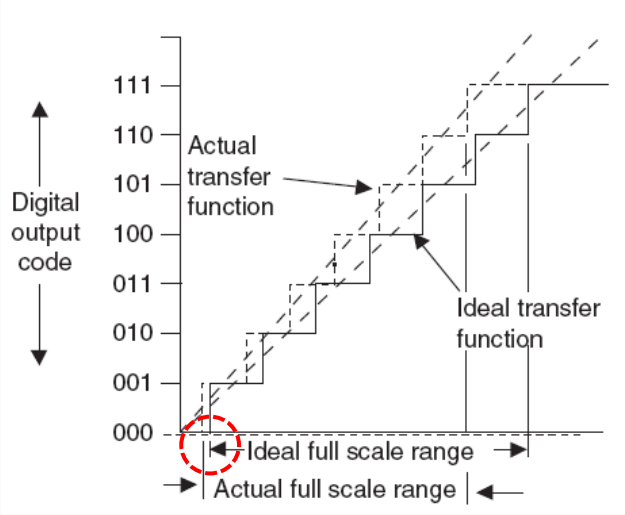


Fig. 15.9 Illustrating offset and gain errors for a 2-bit D/A converter

ADC

Offset error(E_{off})

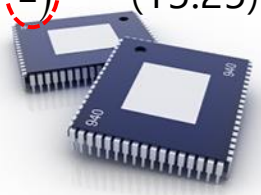
$$E_{off\,(D/A)} = \left.\frac{V_{out}}{V_{LSB}}\right|_{B_{in}=0\ldots0} \qquad (15.22)$$

$$E_{off\,(A/D)} = \frac{\left.V\right|_{B_{in}=0\ldots01}}{V_{LSB}} + \frac{1}{2}LSB \qquad (15.23)$$

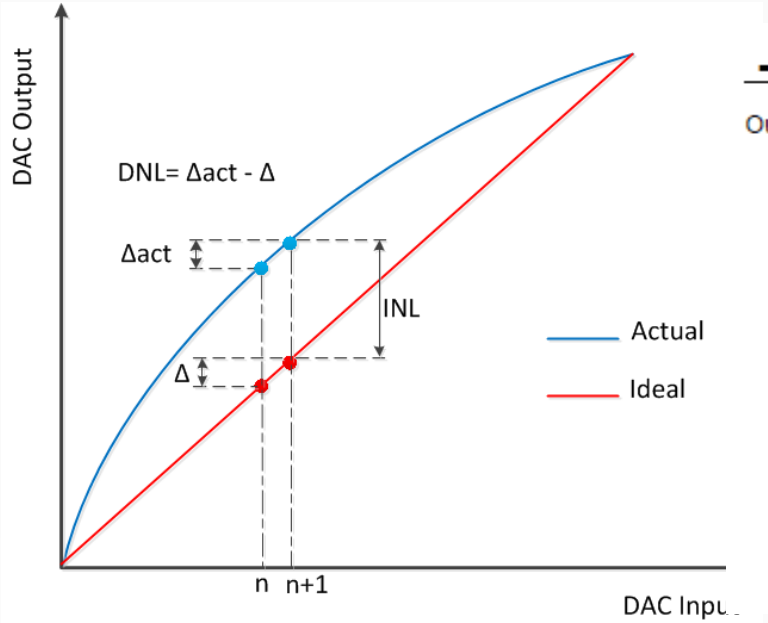
gain error (E_{gain})

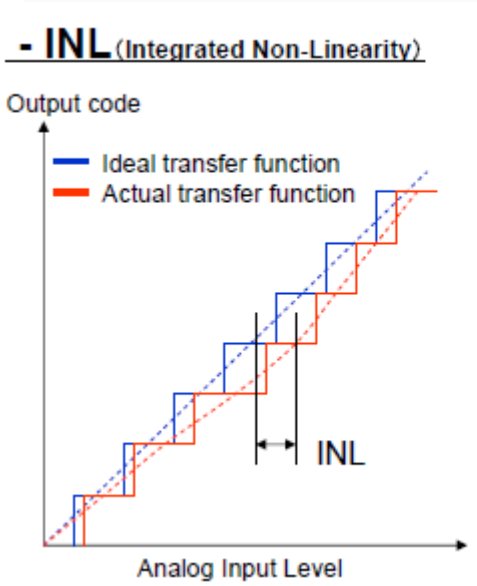
$$E_{off\,(D/A)} = \left(\left.\frac{V_{out}}{V_{LSB}}\right|_{B_{in}=1\ldots1} - \left.\frac{V_{out}}{V_{LSB}}\right|_{B_{in}=0\ldots0}\right) - \left(2^N - 1\right) \qquad (15.24)$$

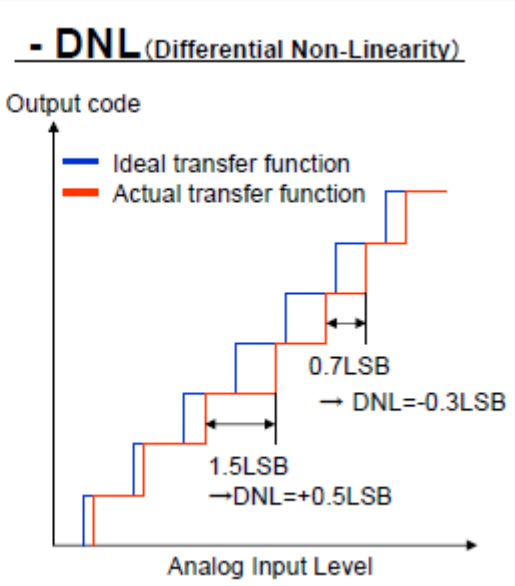
$$E_{off\,(D/A)} = \left(\frac{\left.V\right|_{B_{in}=1\ldots11}}{V_{LSB}} - \frac{\left.V\right|_{B_{in}=0\ldots01}}{V_{LSB}}\right) - \left(2^N + 2\right) \qquad (15.25)$$



INL & DNL







INL for D/A converter

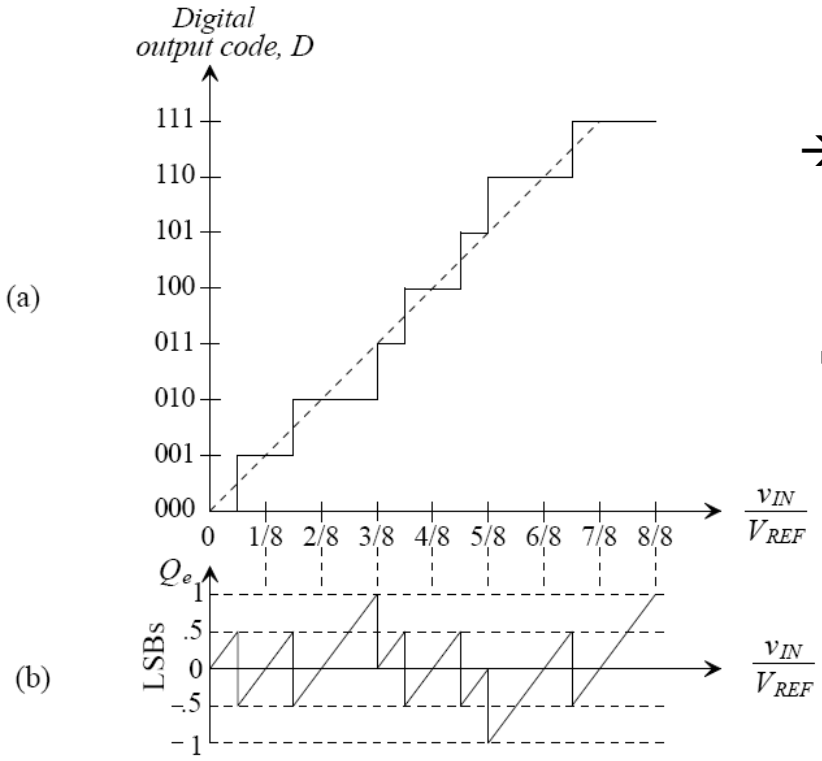
INL (Integral nonlinearity)
= maximum deviation between an actual code transition point and ideal transition point

DNL for D/A converter

DNL (Differential nonlinearity)
= measure of variations in code widths form the ideal code width

Example 3

Calculate the differential nonlinearity of the 3-bit ADC. Draw the quantization error, Q_e, in units of LSBs. Assume that V_{REF}=5V.



DNL_n = Actual step width – Ideal step width

→ ideal step width

$$V_{ideal\ \ step-width} = \frac{1}{2^3} \cdot V_{REF} = 0.625V = 1LSB$$

- Calculate DNL

$DNL_0 = DNL_1 = DNL_4 = 0$

$DNL_2 = 1.5LSB - 1LSB = 0.5LSB$

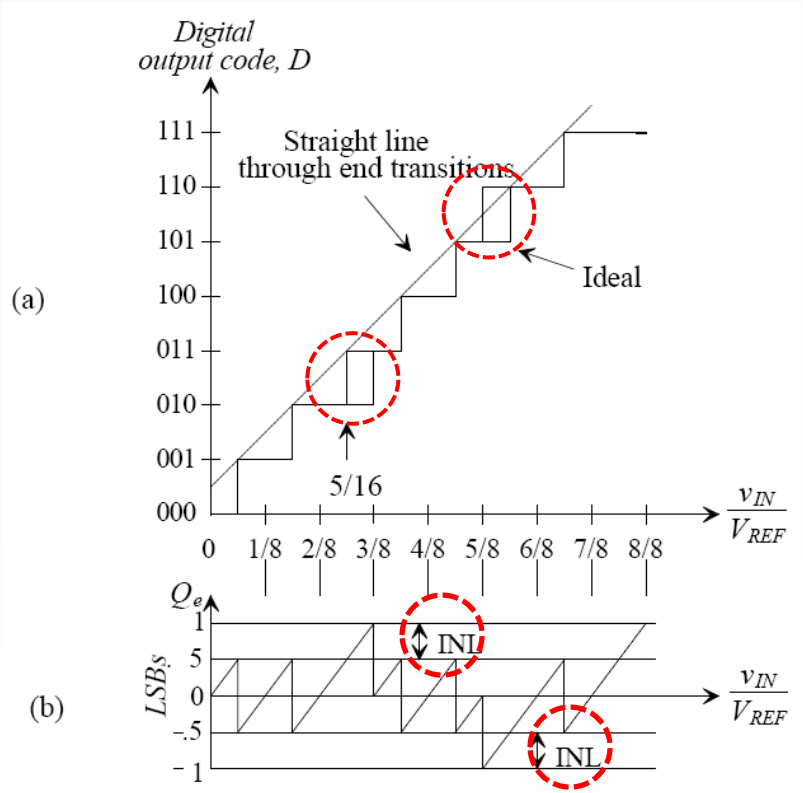
$DNL_3 = 0.5LSB - 1LSB = -0.5LSB$

$DNL_5 = -0.5LSB$, $DNL_6 = 0.5LSB$

$DNL_7 = 0$

Example 4

Calculate the Integral nonlinearity of the 3-bit ADC. Draw the quantization error, Q_e, in units of LSBs. Assume that V_{REF}=5V.



INL = difference between code transition point and straight drawn line

- Calculate INL

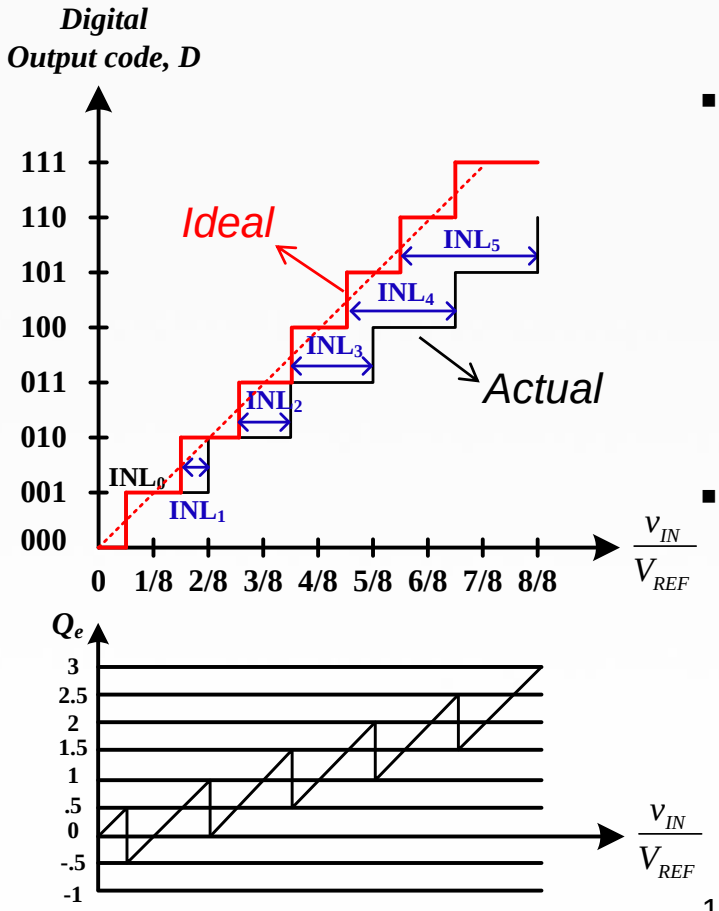
$INL_0 = INL_1 = INL_3 = INL_4 = INL_6 = 0$

$INL_2 = 3/8 – 5/16 = 1/16$ or 0.5LSB

$INL_5 = – 0.5LSB$

Example 5

Calculate the differential & Integral nonlinearity of the 3-bit ADC. Draw the quantization error, Q_e, in units of LSBs. Assume that V_{REF}=5V.



- Calculate DNL

$DNL_0 = 0$

$DNL_1 = DNL_2 = DNL_3 = DNL_4 = DNL_5$
$= 1.5LSB – 1LSB = 0.5LSB$

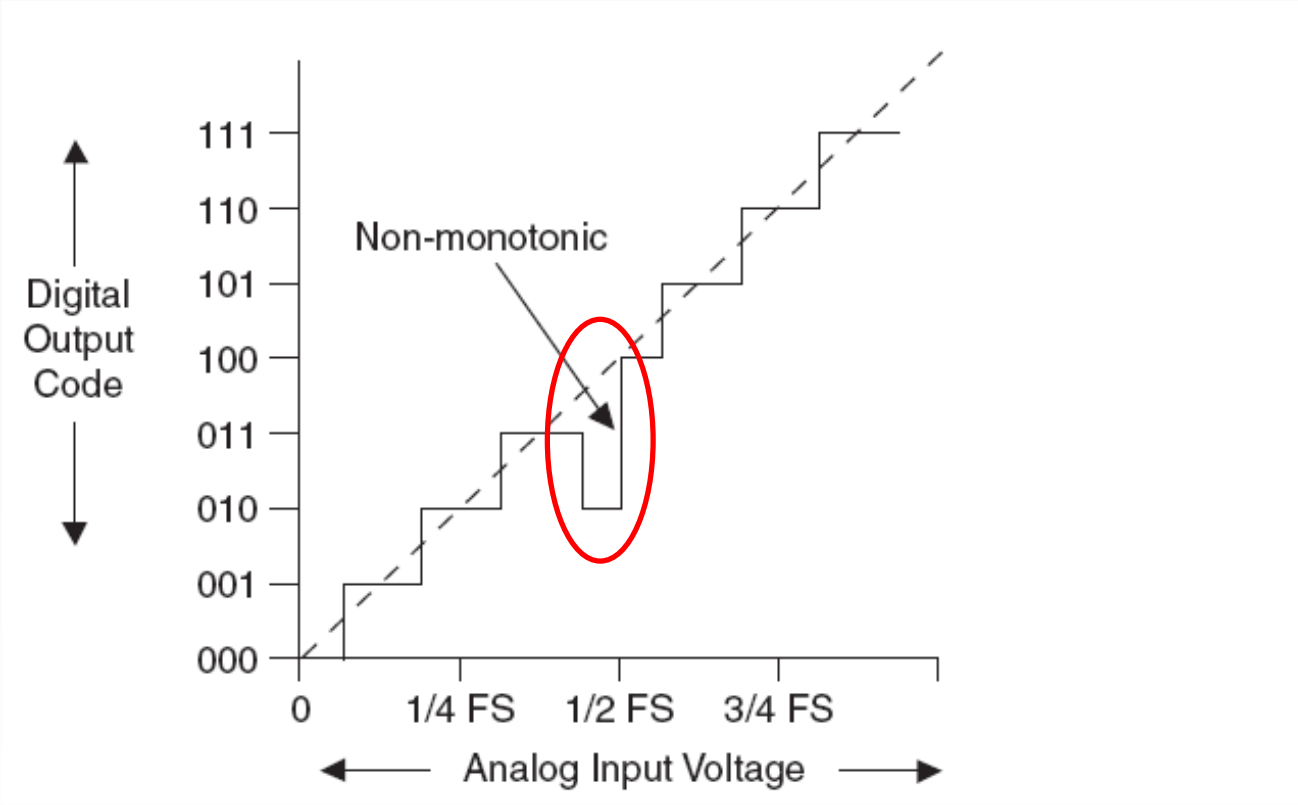
- Calculate INL

$INL_0 = 0$

$INL_1 = 0.5LSB$, $INL_2 = 1LSB$, $INL_3 = 1.5LSB$

$INL_4 = 2LSB$, $INL_5 = 2.5LSB$

Monotonic



If the output code always increases when the input increase the device is called Monotonic

Sampling rate & Resolution