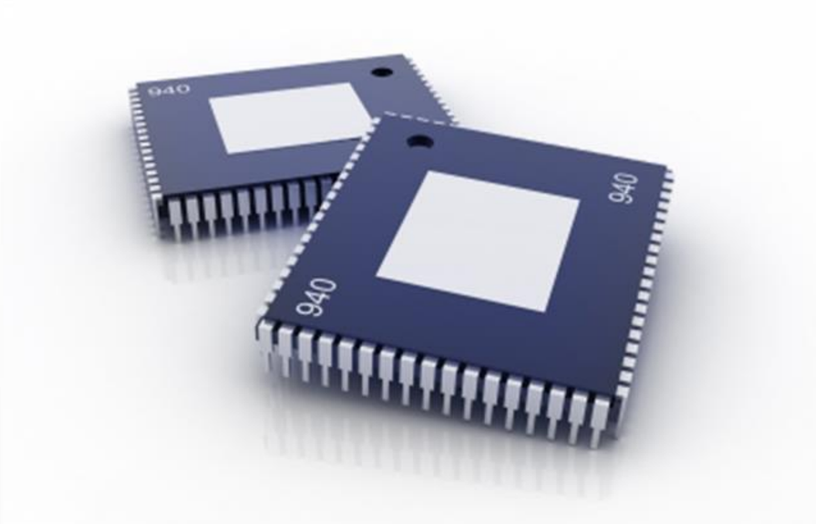


LECTURE 14

Soo-Won Kim

swkim@korea.ac.kr

17. Nyquist-rate A/D converter

17.1 Integrating converters

17.2 Successive-approximation converter

17.3 Algorithmic (or cyclic) A/D converter

17.4 Pipelined A/D converter

17.5 Flash converters

17.6 Two-step A/D converters

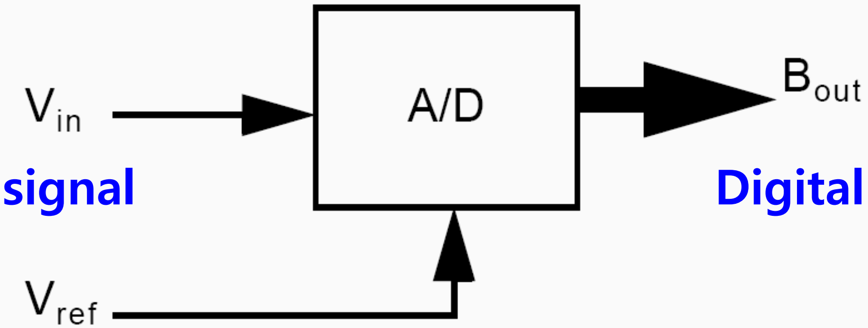
17.7 Interpolating A/D converters

17.8 Folding A/D converters

17.9 Time-interleaved A/D converters

A/D converter basics

Analog signal



Digital signal

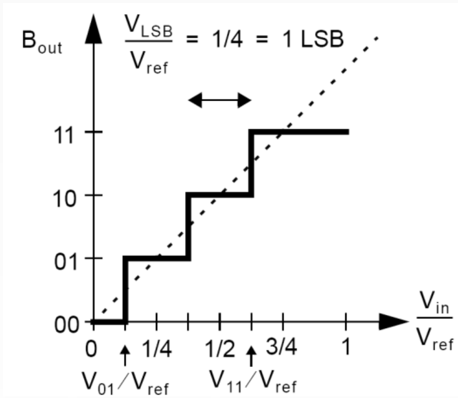
Fig. 15.3 A block diagram representing an A/D converter

- V_{in} : analog signal

$$V_{ref}\left(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}\right)$$

$$= V_{in} \pm V_x$$

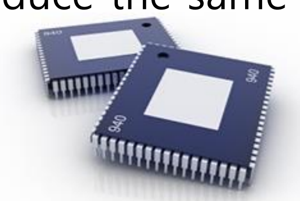
$$-\frac{1}{2}V_{LSB} \le V_x \le \frac{1}{2}V_{LSB} \qquad (15.8)$$



$$-\frac{1}{2}V_{LSB} \le V_x \le \frac{1}{2}V_{LSB}$$

Quantization error(V_{LSB})

Range of input values that produce the same digital output word



Analog to Digital Converter

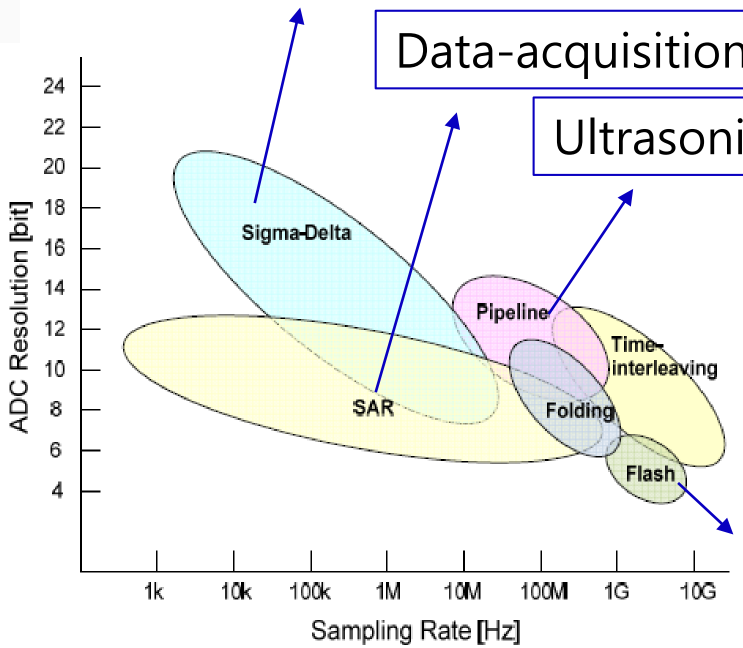
Table 17.1 Different A/D converter architectures

Low-to-Medium Speed, High Accuracy	Medium Speed, Medium Accuracy	High Speed, Low-to-Medium Accuracy
Oversampling(Σ-Δ) Integrating	Successive approximation Algorithmic	Flash Two-step Interpolating Folding Pipelined Time-interleaved

Industrial Measurement, Audio

Data-acquisition applications

Ultrasonic medical imaging



Disk driver

Topology	Conversion rate	Resolution
SAR	<5M samples/s	Up to 18bit
Σ-Δ	<625k samples/s	Up to 24bit
Pipeline	<500M samples/s	Up to 16bit

Integrating converters

Single slope A/D converter

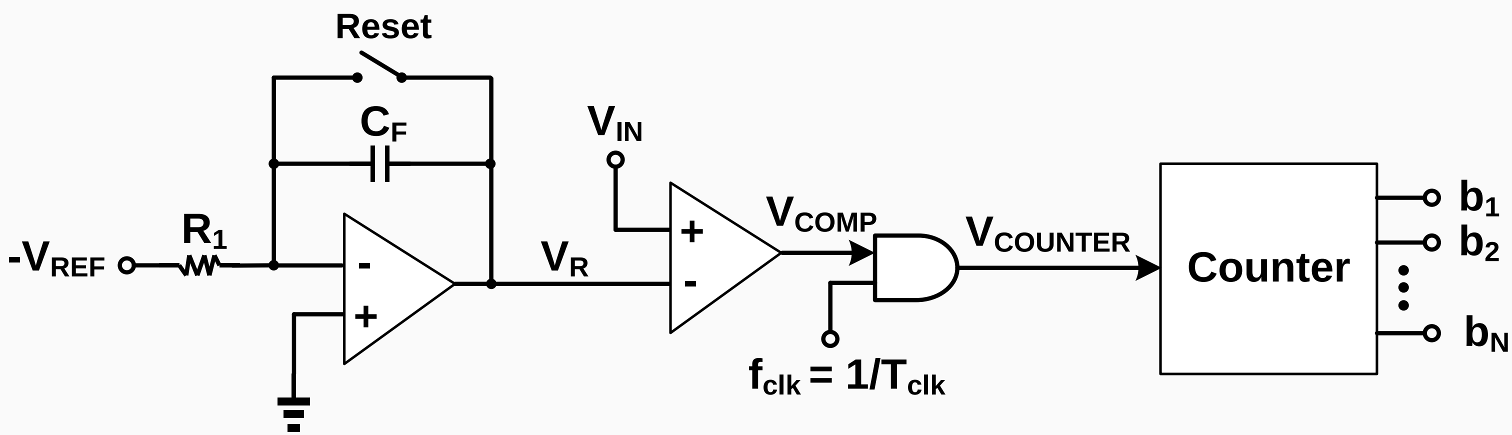
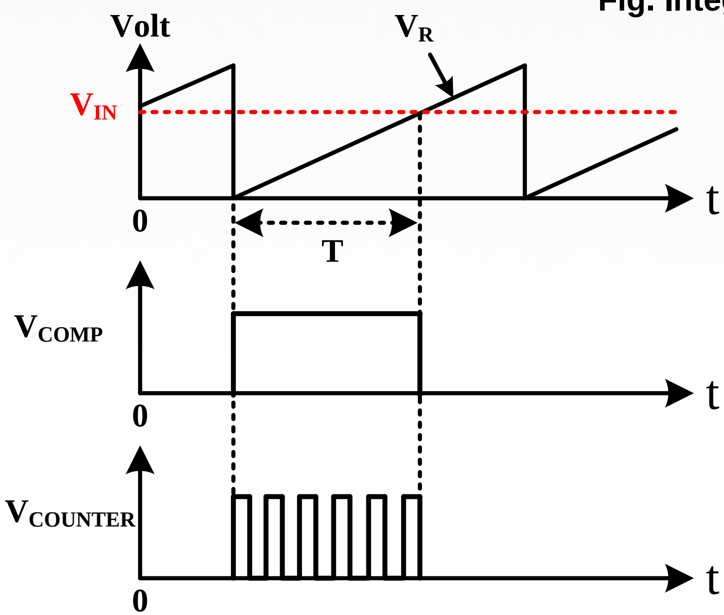


Fig. Integrating (single slope) A/D converter



- Integrating circuit

$$V_R = -\frac{1}{C}\int i\,dt = \frac{1}{C}\frac{V_{REF}}{R}t \qquad (17.2)$$

- $t = T,\ T = N \times T_{clk}$

$$N = \frac{RC}{T_s}\cdot\frac{V_{IN}}{V_{REF}}$$

Depend on the time constant (RC)

Integrating converters

Dual slope A/D converter

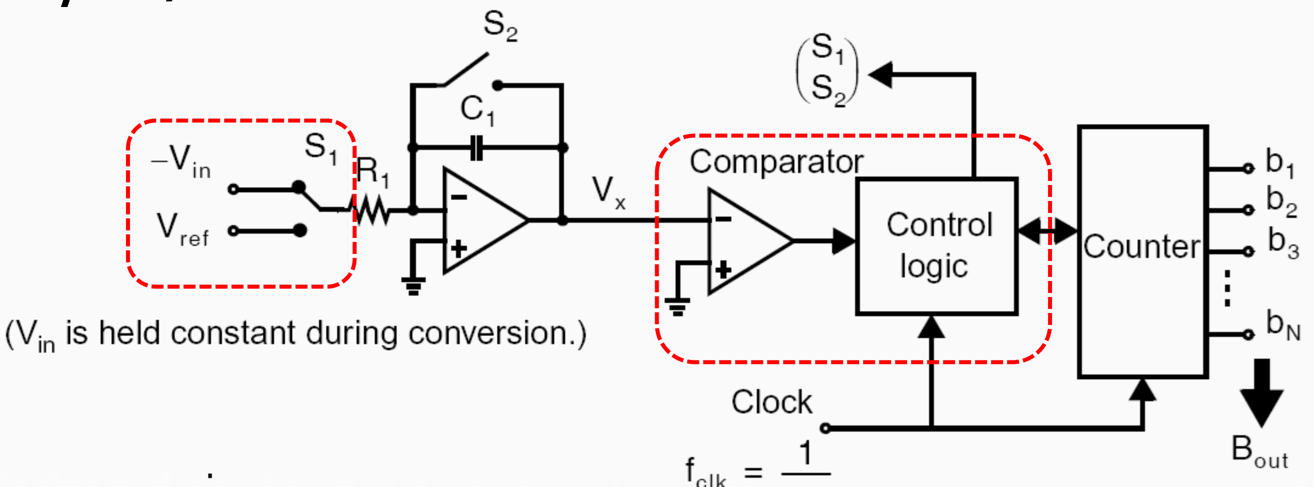


Fig. 17.1 Integrating (dual slope) A/D converter

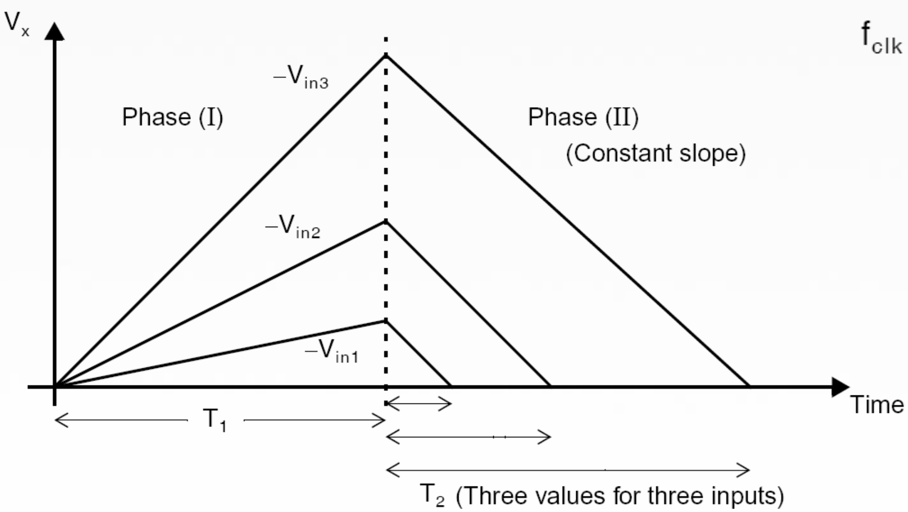


Fig. 17.2 Operation of the integrating converter for three different input voltages

- $V_x = 0$ when $t = T_1 + T_2$,

$$0 = \frac{V_{in} T_1}{R_1 C_1} - \frac{V_{ref} T_2}{R_1 C_1} \qquad (17.6)$$

$$\Rightarrow \quad T_2 = T_1 \left(\frac{V_{in}}{V_{ref}} \right) \qquad (17.7)$$

Not depend on the time constant (RC)

Example 1

Find the value of C1 of a 16-bit integrating A/D converter. Assume that V_X=5V, V_{in}=3V, T_1=1/50 Hz, R_1=100MΩ

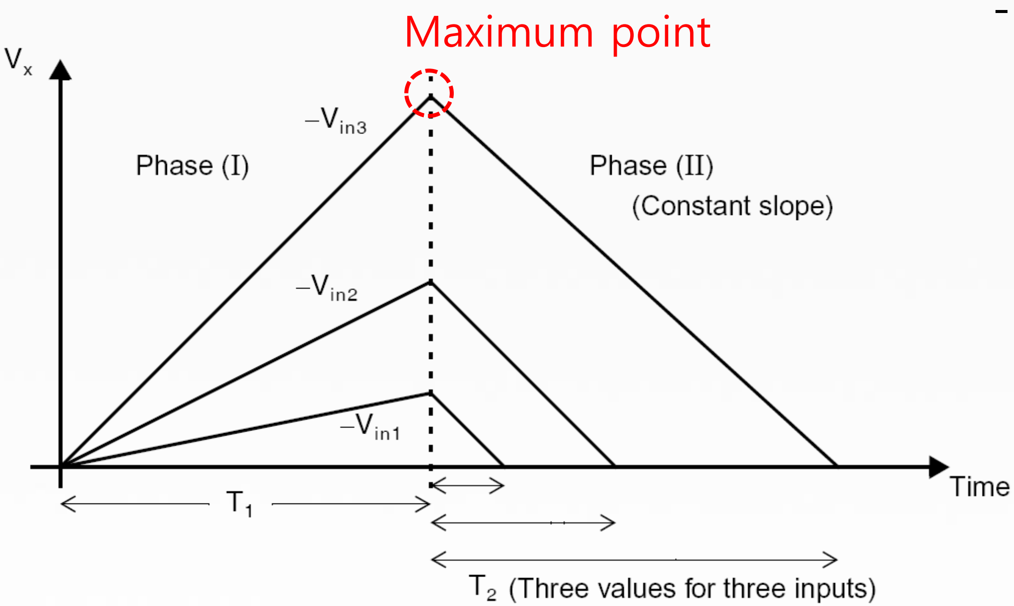


Fig. 17.2 Operation of the integrating converter for three different input voltages

- At maximum point,

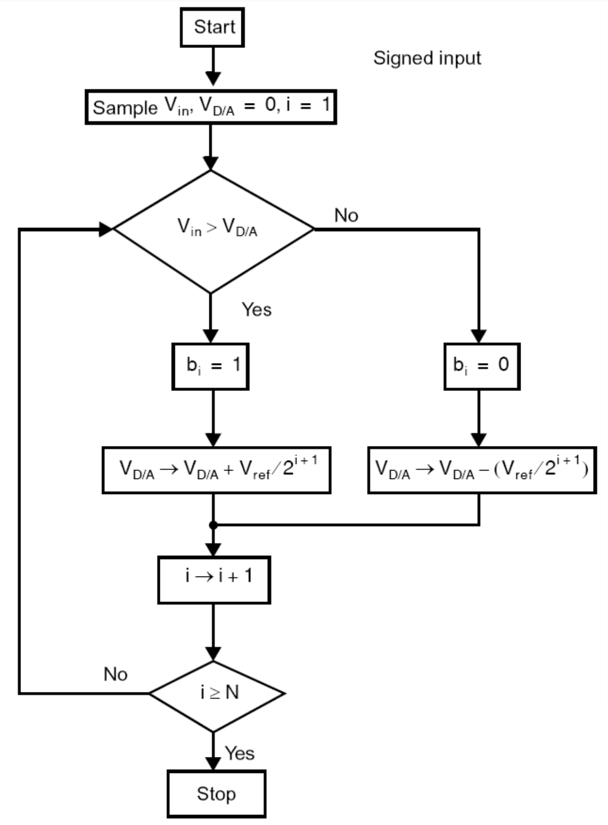
$$V_{x,\mathbf{max}} = \frac{V_{in,\mathbf{max}}}{R_1 C_1} \cdot T_1 \qquad (17.14)$$

$$C_1 = \frac{1}{R_1} \frac{V_{in,\mathbf{max}}}{V_{x,\mathbf{max}}} \cdot T_1 \qquad (17.16)$$

$$\Rightarrow C_1 = \frac{1}{100M} \frac{3}{5} \cdot 20m$$

$$= 120pF$$

D/A-based successive approximation



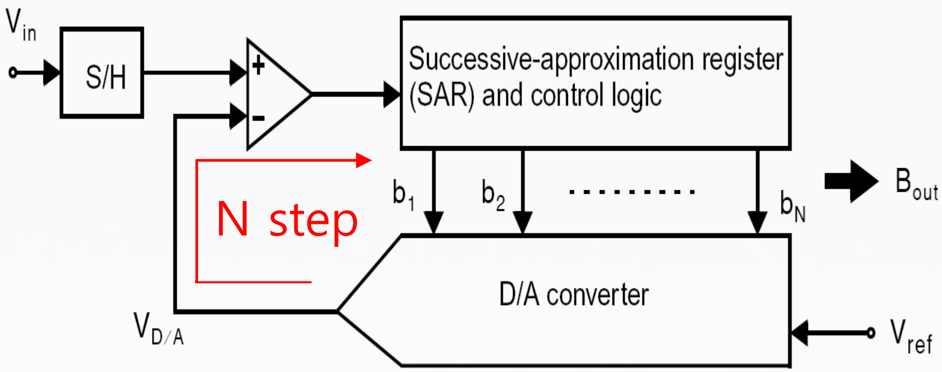


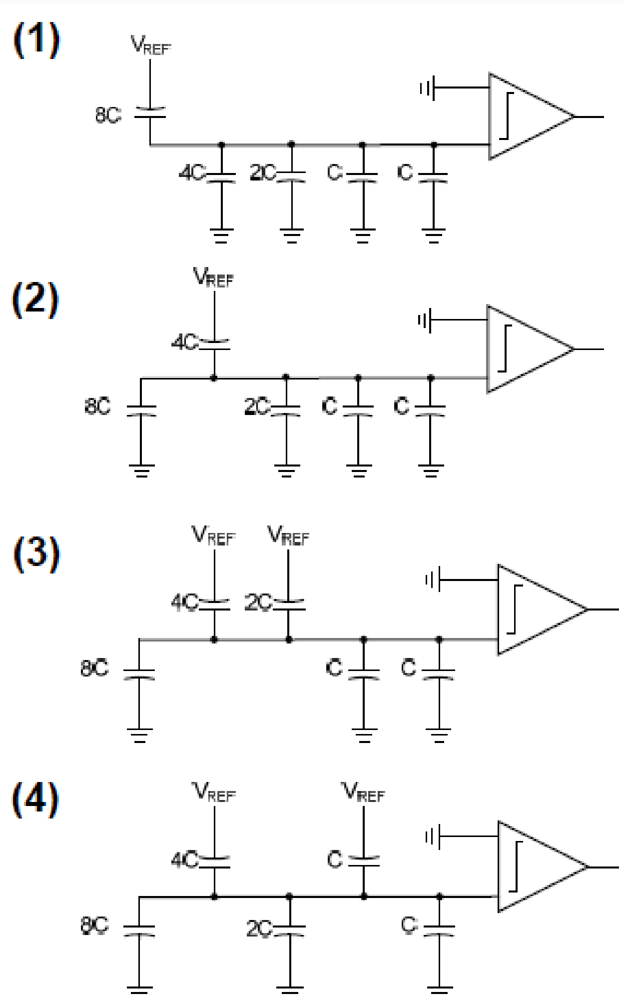
Fig. 17.4 Flow graph for the successive-approximation approach

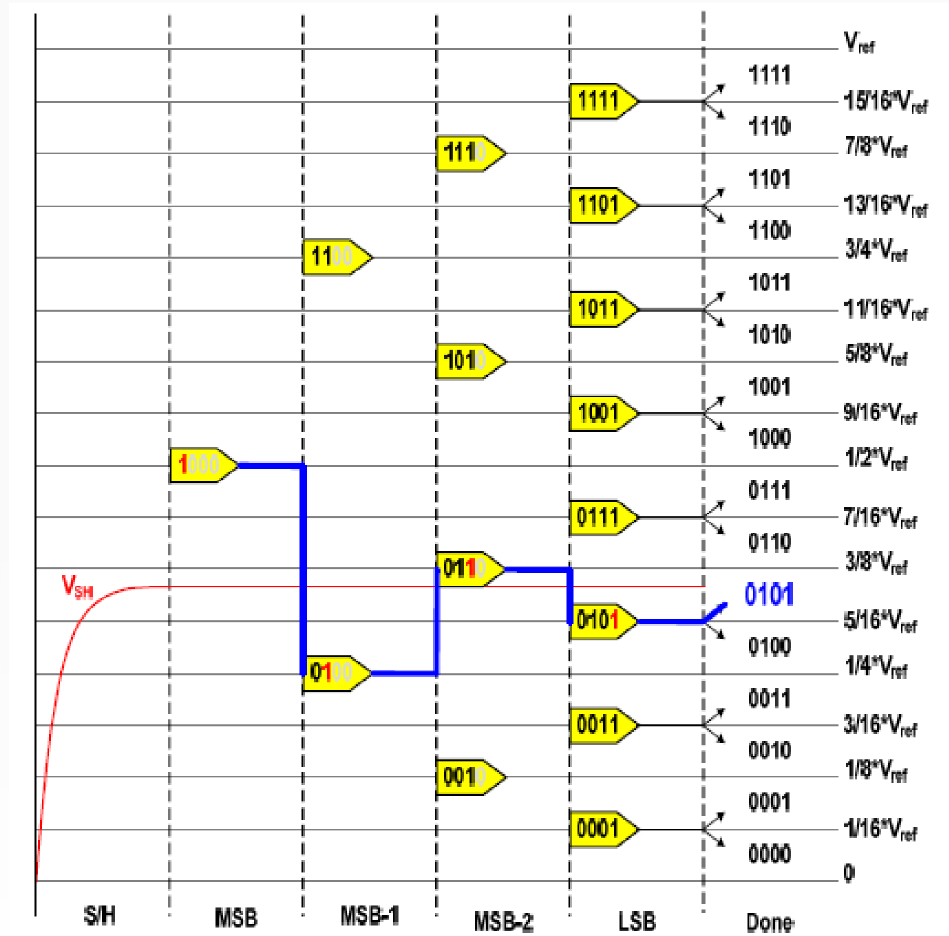
Fig. 17.5 D/A converter-based successive-approximation converter

Need a S/H, D/A converter

Requires N step for N-bit converter

Successive-approximation converters





Charge-redistribution A/D

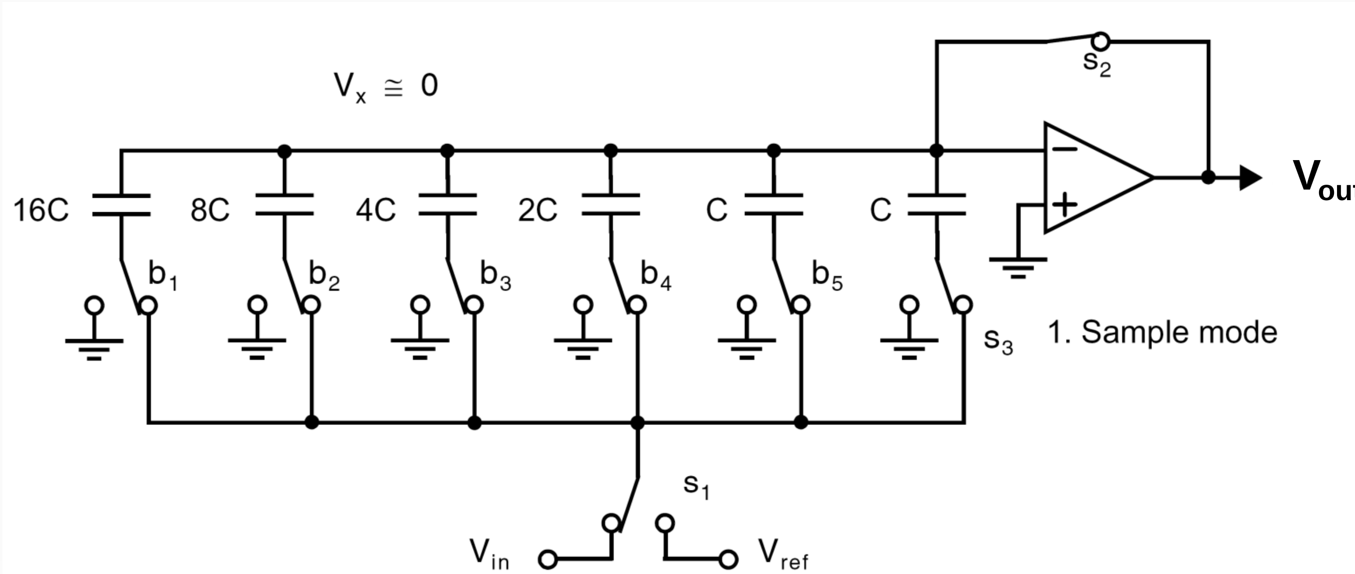
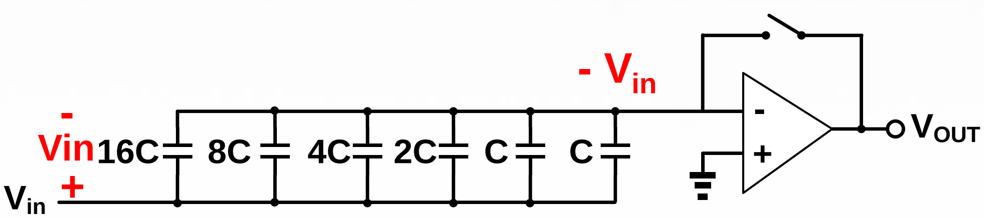
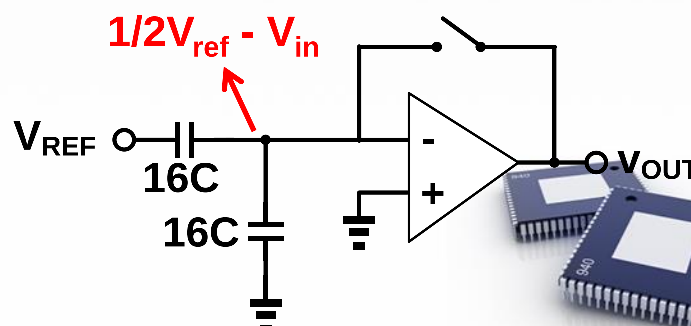


Fig. 17.7 A 5-bit charge-redistribution A/D converter

① S_1 on(V_{in}), b_{54321} = 11111, S3 on(V_{in})
→ S/H mode



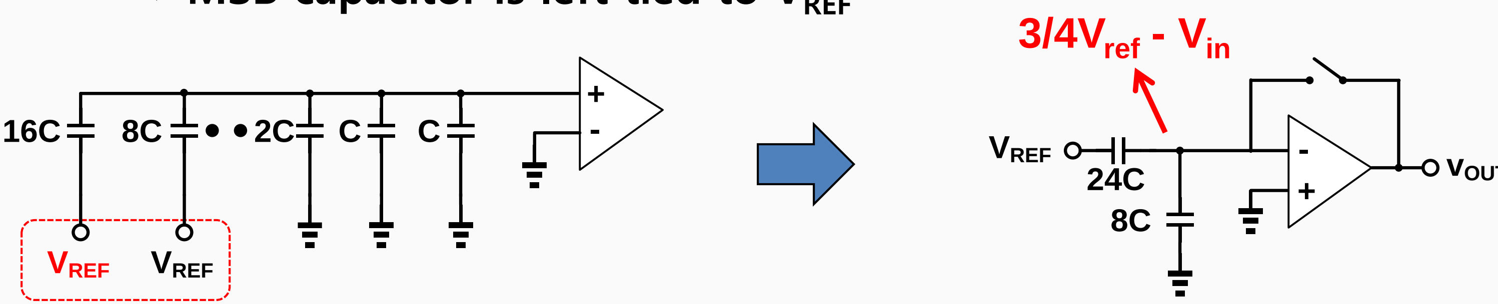
② S_1 off(V_{ref}), b_{12345} = 10000, S3 off(gnd)
→ comparator (MSB)



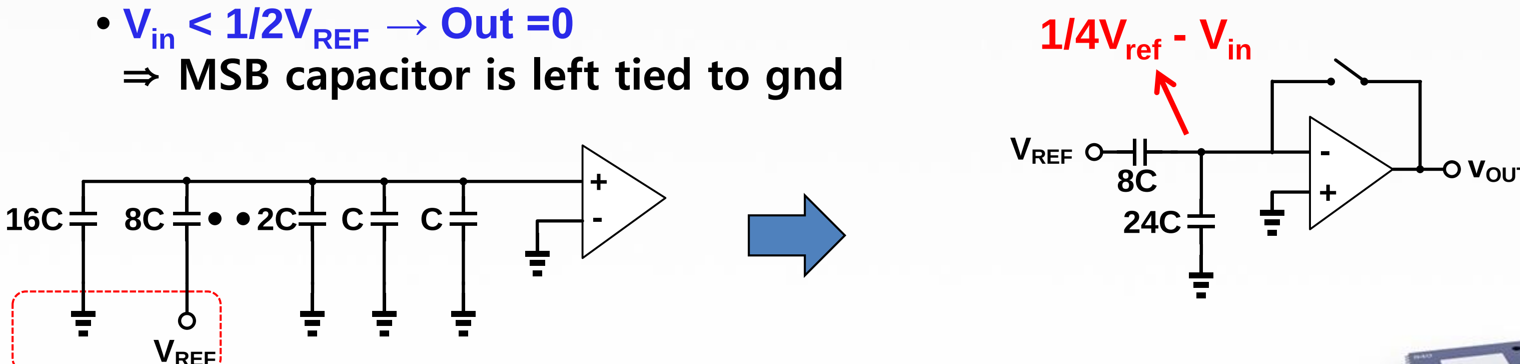
Charge-redistribution A/D

③ MSB-1

- $V_{in} > 1/2V_{REF} \rightarrow$ Out =1
  ⇒ MSB capacitor is left tied to V_{REF}



- $V_{in} < 1/2V_{REF} \rightarrow$ Out =0
  ⇒ MSB capacitor is left tied to gnd



Example 2

Find V_x during the operation of the 5-bit charge-redistribution converter.
Assume that V_{in} = 1.23V, V_{ref} = 5V.

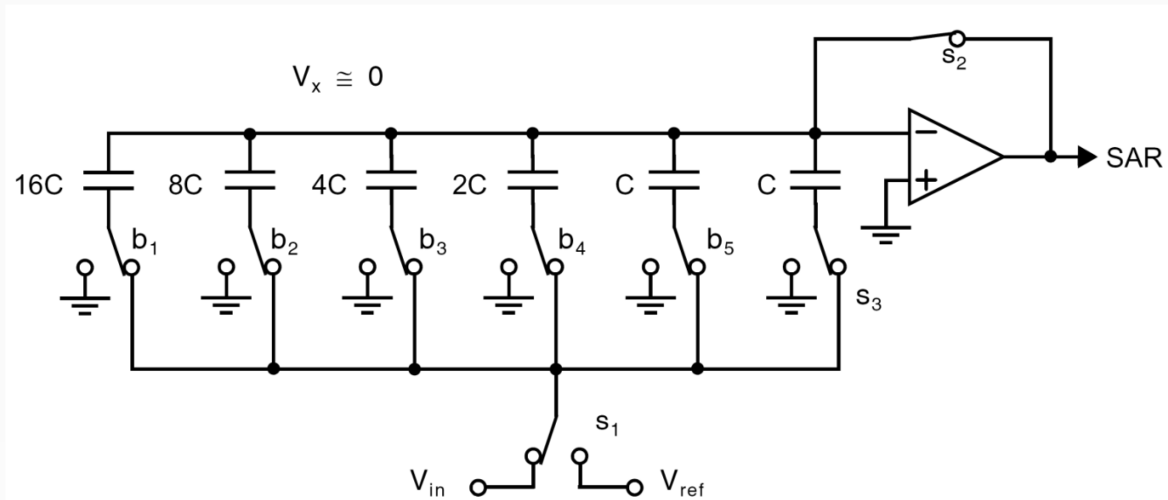
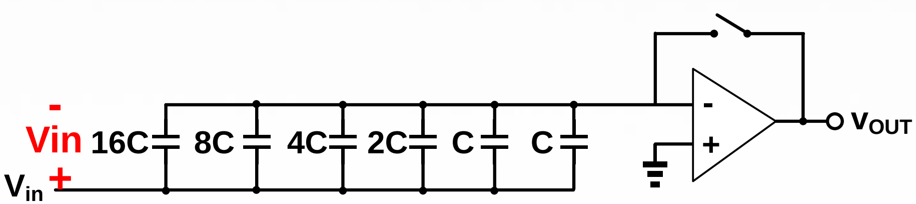


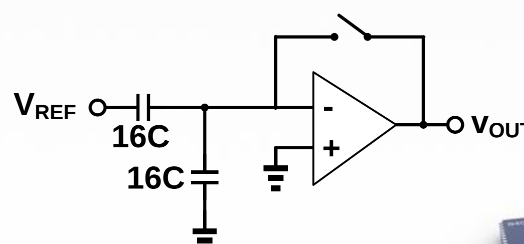
Fig. 17.7 A 5-bit charge-redistribution A/D converter

- Sample mode



$$V_x = (-V_{in}) = -1.23V$$

- b_{12345} = 10000 (MSB) -> b_1=0

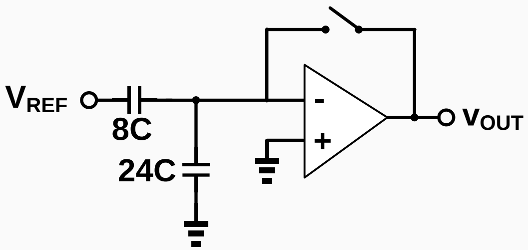


$$V_x = -1.23 + \frac{16}{32} \times 5 = 1.21V > 0$$

Example 2(Cont.)

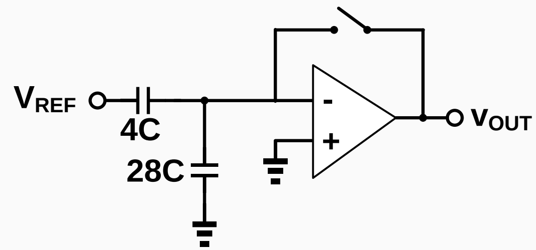
Find V_x during the operation of the 5-bit charge-redistribution converter. Assume that V_{in} = 1.23V, V_{ref} = 5V.

- b_{12345} = 01000 -> b_2=0



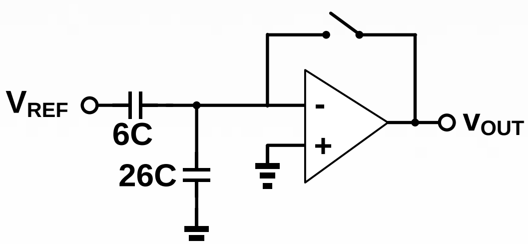
$$V_x = -1.23 + \frac{8}{32} \times 5 = 0.02V > 0$$

- b_{12345} = 00100 -> b_3=1



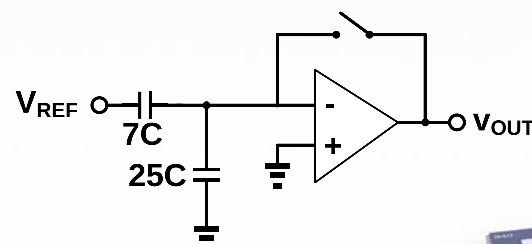
$$V_x = -1.23 + \frac{4}{32} \times 5 = -0.605V < 0$$

- b_{12345} = 00110 -> b_4=1



$$V_x = -1.23 + \frac{6}{32} \times 5 = -0.293V < 0$$

- b_{12345} = 00111 -> b_4=1



$$V_x = -1.23 + \frac{7}{32} \times 5 = -0.136V < 0$$