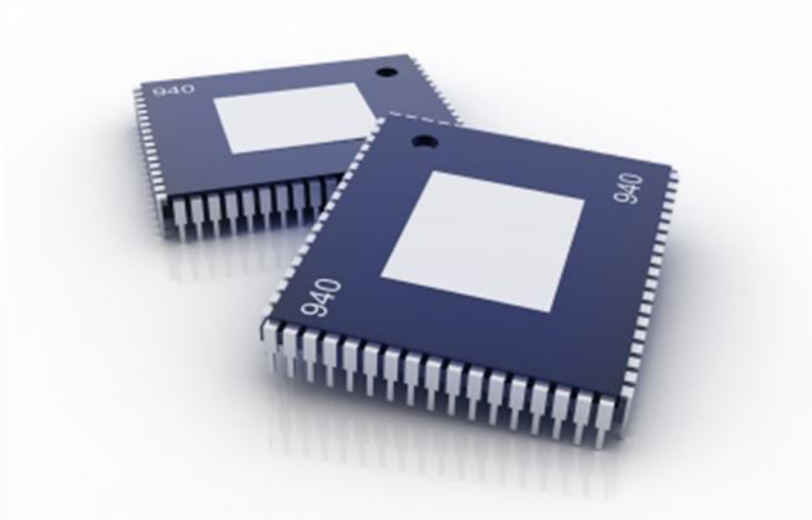

LECTURE 16

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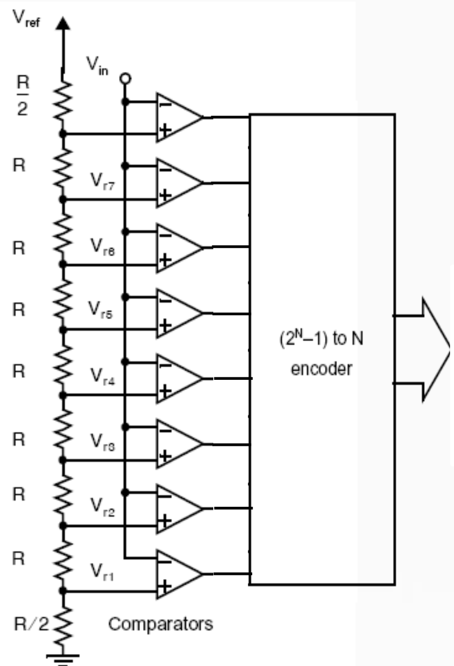
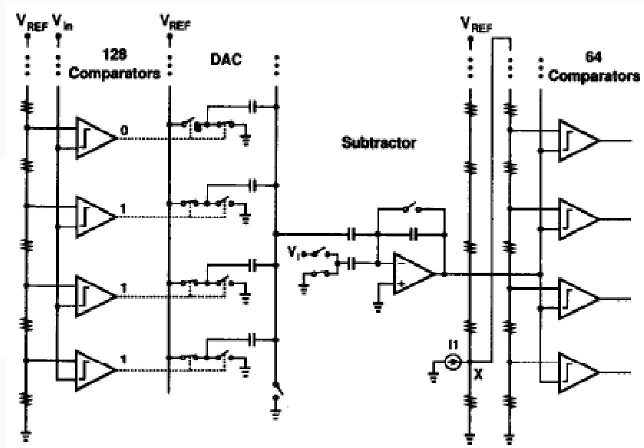
Lecture 16

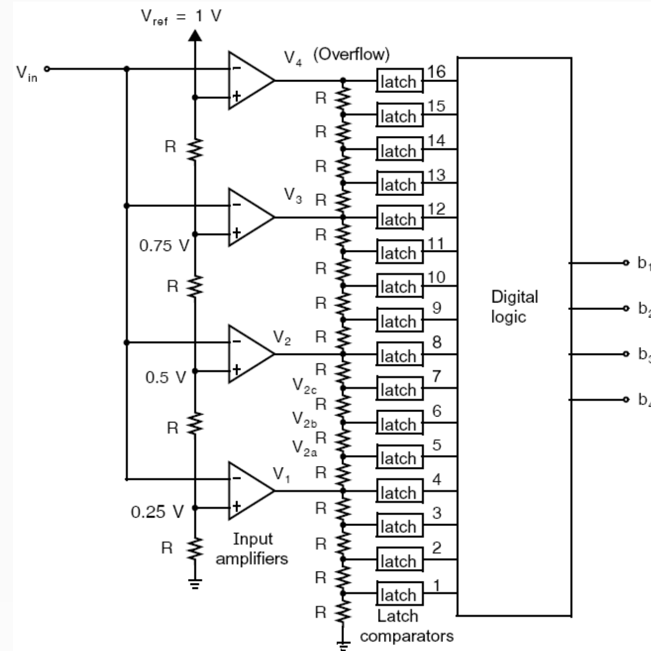
17. Nyquist-rate A/D converter

17.1 Integrating converters
17.2 Successive-approximation converter
17.3 Algorithmic (or cyclic) A/D converter
17.4 Pipelined A/D converter
17.5 Flash converters
17.6 Two-step A/D converters
17.7 Interpolating A/D converters
17.8 Folding A/D converters
17.9 Time-interleaved A/D converters

ADC speed







Topology	Conversion rate	Resolution
Flash	<5G samples/s	Up to 8bit
Two-step	<100M samples/s	Up to 16bit
interpolating	<3G samples/s	Up to 6bit

Flash converters

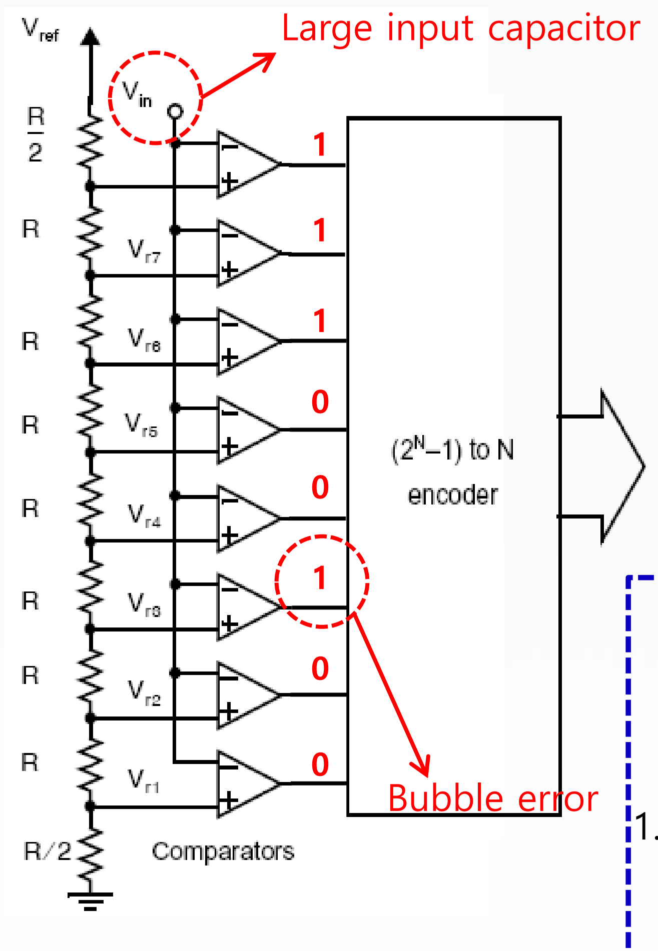
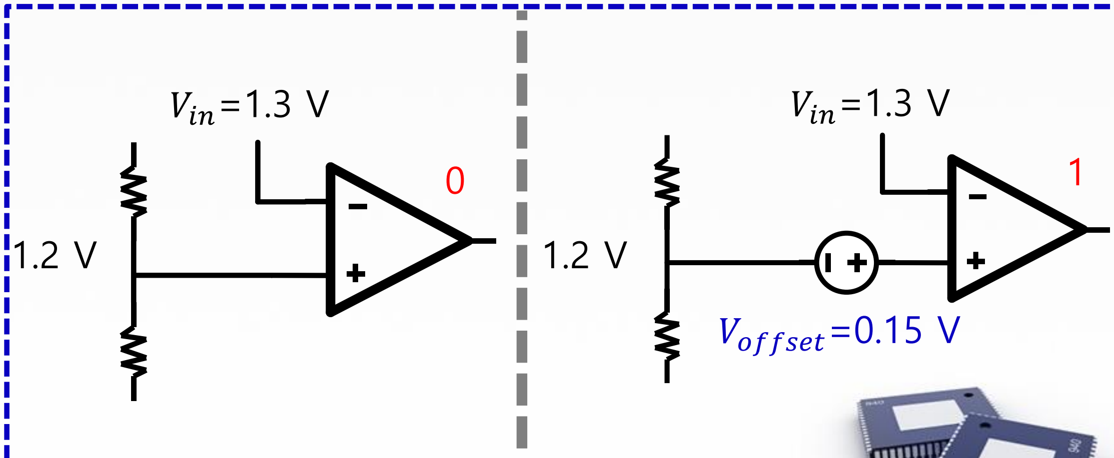


Fig. A 3-bit flash A/D converter

- High-speed
- Monotonic(thermometer code)

- Area & Power consumption
- Require 2^N resistors & comparator
- Large input capacitor
- **Bubble error**



Example 1

Find the digital output during the operation of the 3-bit flash A/D converter.
Assume that V_{in} = 1.23V, 2.4V, 3.6V, V_{ref} = 5V.

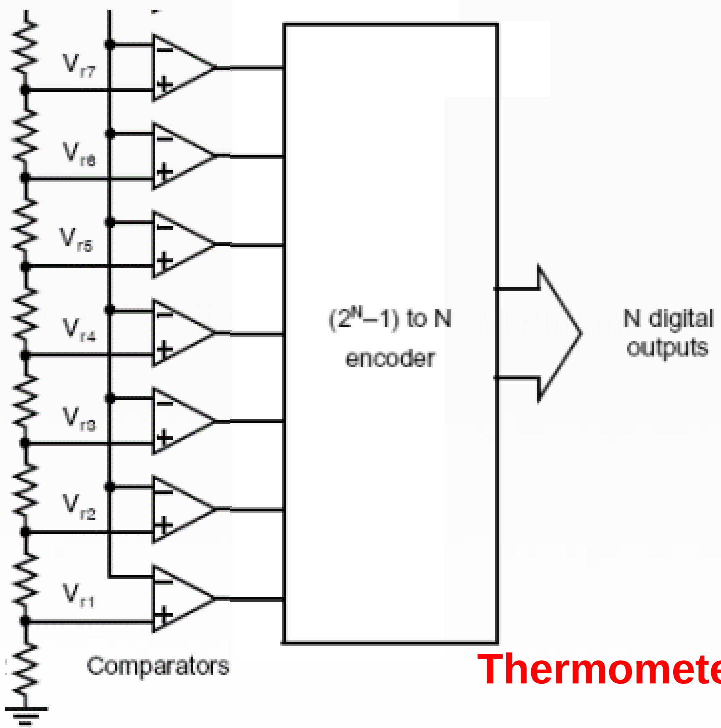


Fig. A 3-bit flash A/D converter

$$V_{r1} = \frac{0.5\cdot R}{8\cdot R}\times V_{ref} = 0.3125V \qquad V_{r5} = \frac{4.5\cdot R}{8\cdot R}\times V_{ref} = 2.8125V$$

$$V_{r2} = \frac{1.5\cdot R}{8\cdot R}\times V_{ref} = 0.9375V \qquad V_{r6} = \frac{5.5\cdot R}{8\cdot R}\times V_{ref} = 3.4375V$$

$$V_{r3} = \frac{2.5\cdot R}{8\cdot R}\times V_{ref} = 1.5625V \qquad V_{r7} = \frac{6.5\cdot R}{8\cdot R}\times V_{ref} = 4.0625V$$

$$V_{r4} = \frac{3.5\cdot R}{8\cdot R}\times V_{ref} = 2.1875V \qquad V_{r8} = \frac{7.5\cdot R}{8\cdot R}\times V_{ref} = 4.6875V$$

	- V_{in} = 1.23V	- V_{in} = 2.4V	- V_{in} = 3.6V
	$V_{r2} < V_{in} < V_{r3}$	$V_{r4} < V_{in} < V_{r5}$	$V_{r6} < V_{in} < V_{r7}$
Thermometer	00000011	00001111	00111111
	↓	↓	↓
Binary	010	100	110

Flash converters

Bubble error removal

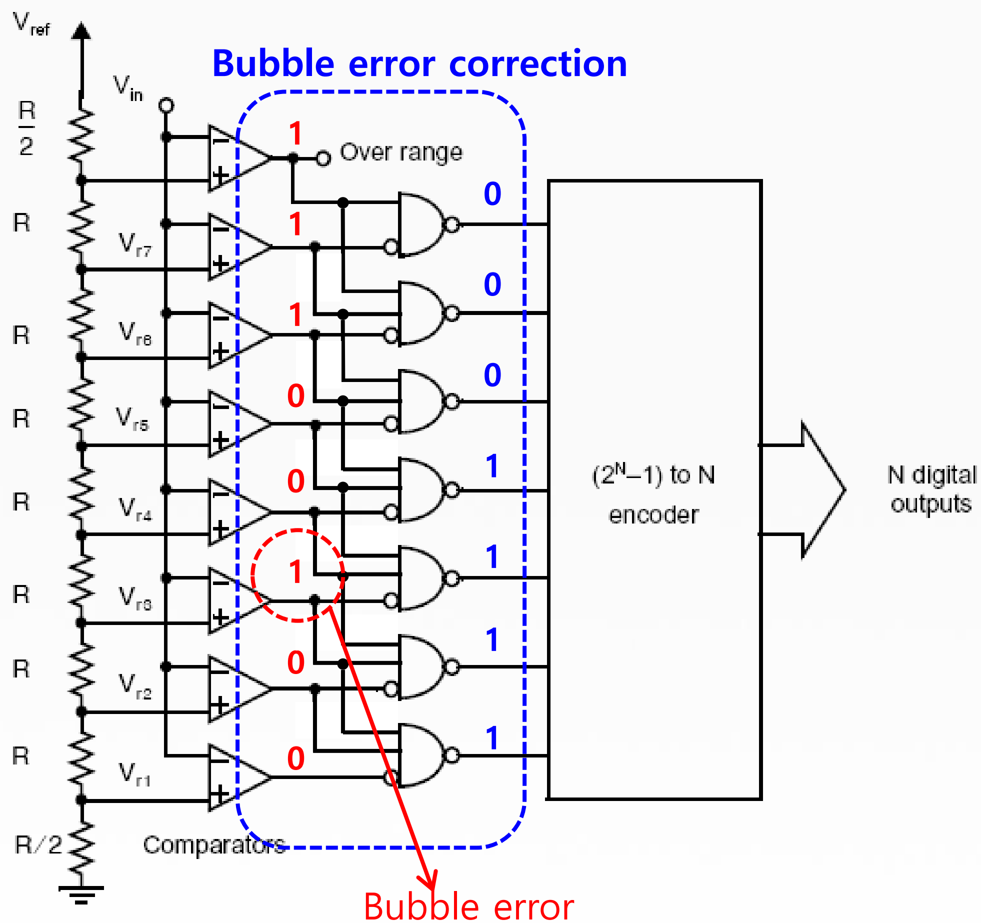


Fig. 17.24 A 3-bit flash A/D converter

Two-step A/D converters

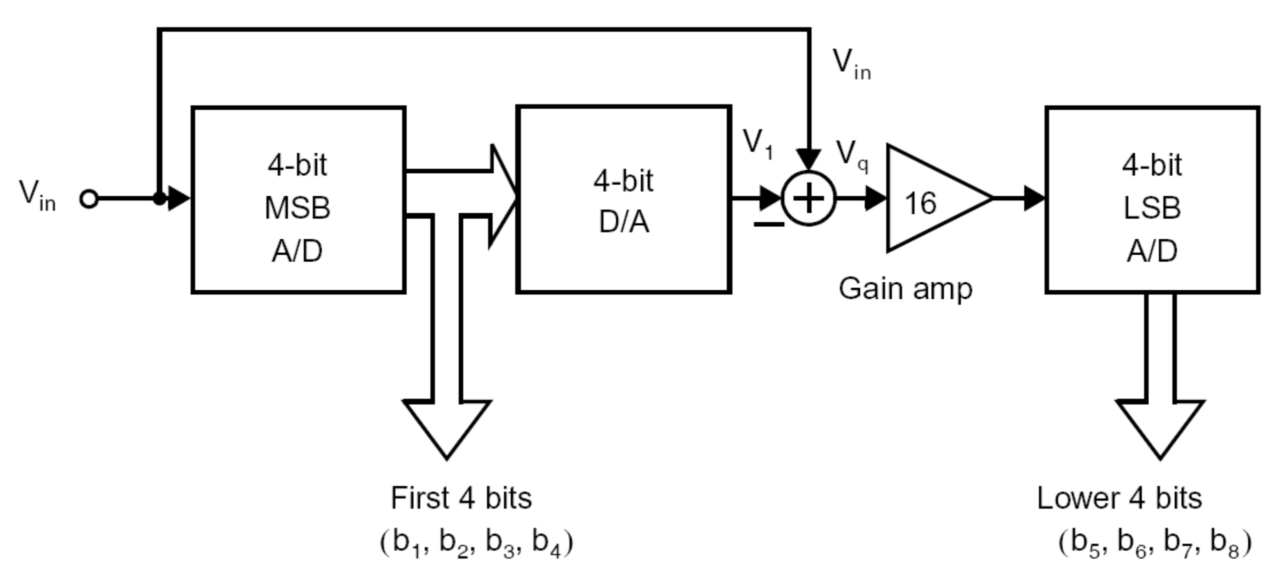


Fig. 17.29 An 8-bit two-step A/D converter

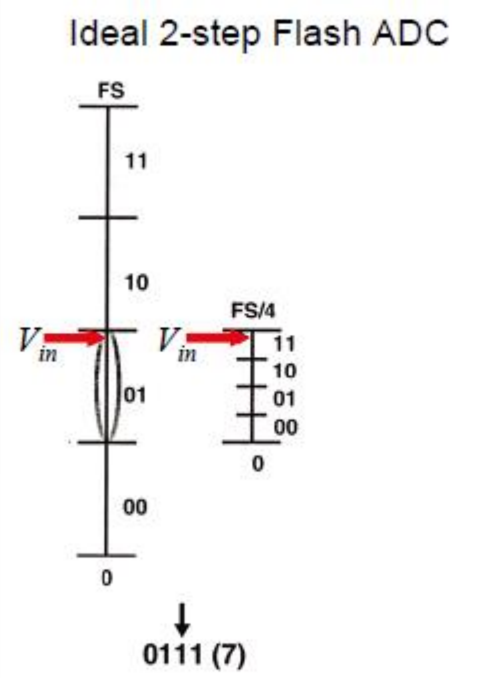
- Area & power consumption ↓
  Reduce the number of comparators

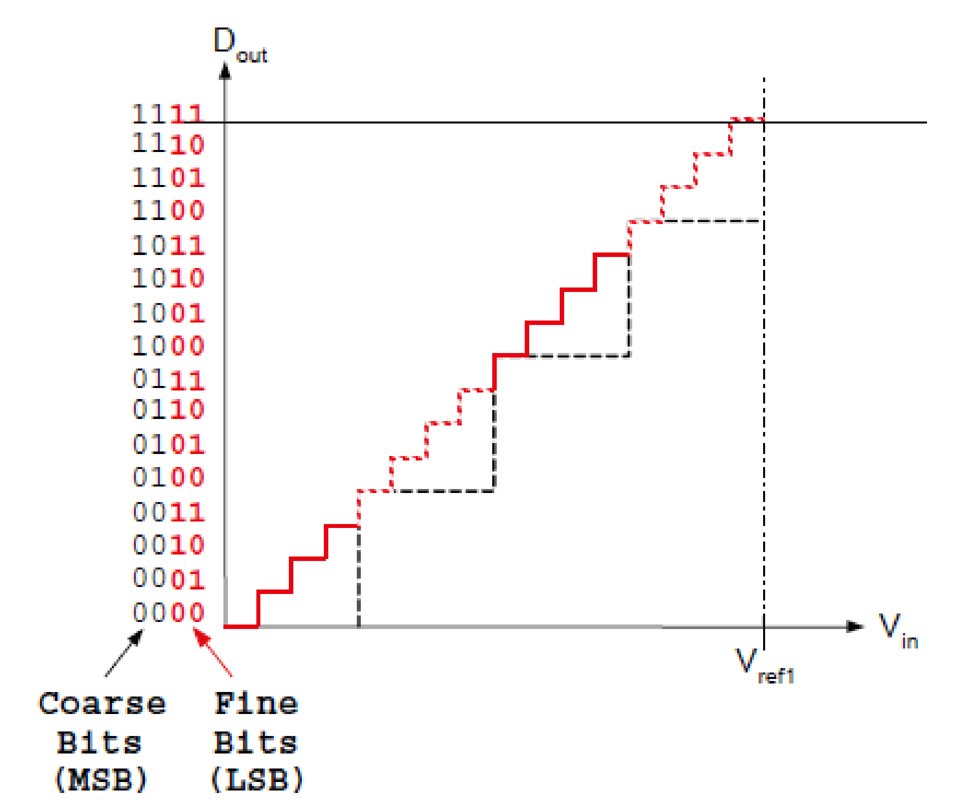
  Ex) 8-bit A/D converter

Flash ADC	Two-step ADC
Comparator : $2^8 = 256$	Comparator : $2 \times 2^4 = 32$

- Speed limitation by bandwidth & settling time of gain amp
  Require accurate gain amp

Two-step A/D converters (Two-step Flash ADC)





Example 2

Find the digital output during the operation of the 4-bit two-step A/D converter(flash ADC). Assume that V_{in} = 1.23V, 3.6V, V_{ref} = 5V.

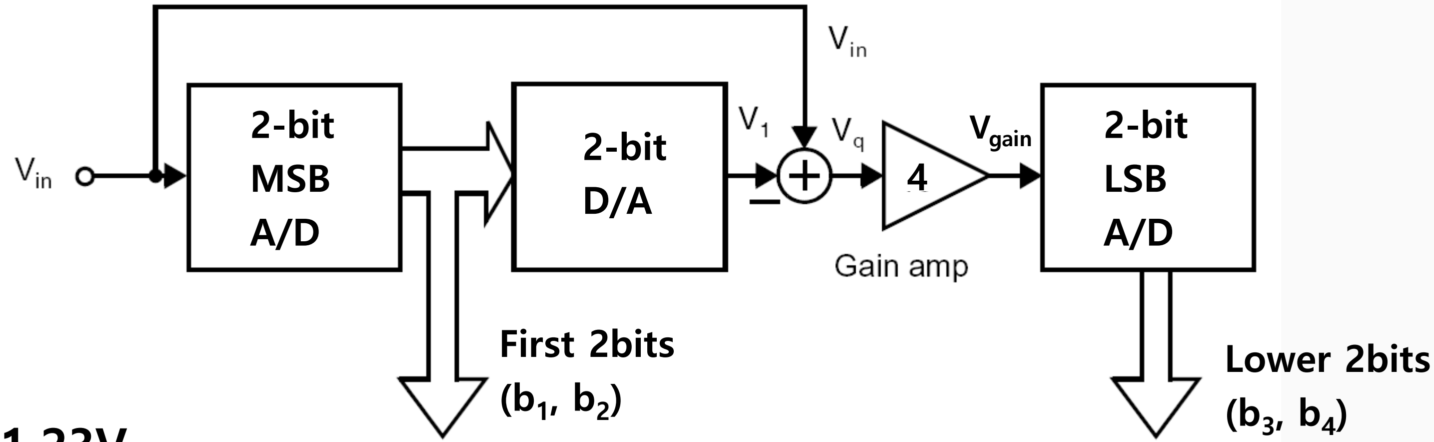


Fig. 17.29 An 4-bit two-step A/D converter

- Vin = 1.23V

$$V_{r1} = \frac{1 \cdot R}{4 \cdot R} \times V_{ref} = 1.25V$$

$$V_{r2} = \frac{2 \cdot R}{4 \cdot R} \times V_{ref} = 2.5V$$

$$V_{r3} = \frac{3 \cdot R}{4 \cdot R} \times V_{ref} = 3.75V$$

- First 2bits

$$V_{in} < V_{r1}$$

$$\downarrow$$

$$b_1, b_2 = 0,0$$

$$\downarrow$$

$$V_1 = 0V$$

$$V_q = V_{in} - V_1 = 1.23 - 0 = 1.23$$

$$\downarrow$$

$$V_{gain} = 4 \cdot 1.23 = 4.92V$$

- Lower 2bits

$$V_{gain} > V_{r3}$$

$$\downarrow$$

$$b_3, b_4 = 1,1$$

Example 2(Cont.)

Find the digital output during the operation of the 4-bit two-step A/D converter(flash ADC). Assume that V_{in} = 1.23V, 3.6V, V_{ref} = 5V.

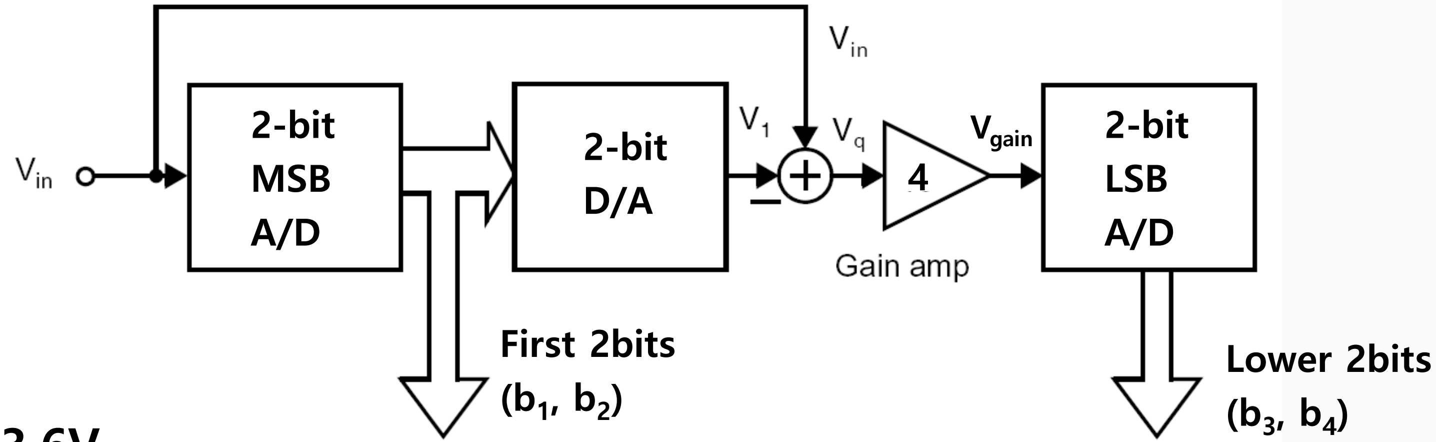


Fig. 17.29 An 4-bit two-step A/D converter

- Vin = 3.6V

$$V_{r1} = \frac{1 \cdot R}{4 \cdot R} \times V_{ref} = 1.25V$$

$$V_{r2} = \frac{2 \cdot R}{4 \cdot R} \times V_{ref} = 2.5V$$

$$V_{r3} = \frac{3 \cdot R}{4 \cdot R} \times V_{ref} = 3.75V$$

- First 2bits

$$V_{r2} < V_{in} < V_{r3}$$
$$\downarrow$$
$$b_1, b_2 = 1, 0$$
$$\downarrow$$
$$V_1 = 2.5V$$

$$V_q = V_{in} - V_1 = 3.6 - 2.5 = 1.1V$$
$$\downarrow$$
$$V_{gain} = 4 \cdot 1.1 = 4.4V$$

- Lower 2bits

$$V_{gain} > V_{r3}$$
$$\downarrow$$
$$b_3, b_4 = 1, 1$$

Example 3

If the gain of gain amp is 3.4, Find the digital output during the operation of the 4-bit two-step A/D converter(flash ADC). Assume that V_{in} = 3.6V, V_{ref} = 5V.

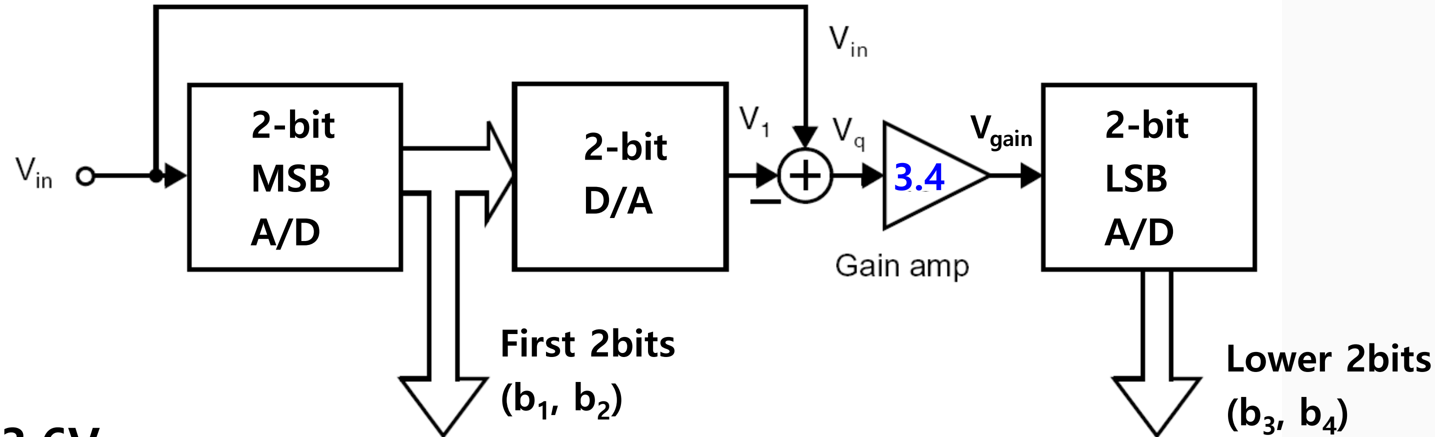


Fig. 17.29 An 4-bit two-step A/D converter

- Vin = 3.6V

$$V_{r1} = \frac{1 \cdot R}{4 \cdot R} \times V_{ref} = 1.25V$$

$$V_{r2} = \frac{2 \cdot R}{4 \cdot R} \times V_{ref} = 2.5V$$

$$V_{r3} = \frac{3 \cdot R}{4 \cdot R} \times V_{ref} = 3.75V$$

- First 2bits

$$V_{r2} < V_{in} < V_{r3}$$

$$\downarrow$$

$$b_1, b_2 = 1, 0$$

$$\downarrow$$

$$V_1 = 2.5V$$

$$V_q = V_{in} - V_1 = 3.6 - 2.5 = 1.1V$$

$$\downarrow$$

$$V_{gain} = 3.4 \cdot 1.1 = 3.74V$$

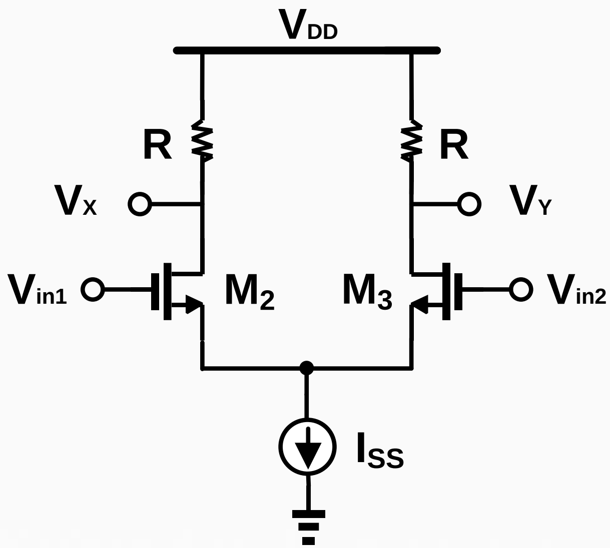
- Lower 2bits

$$V_{r2} < V_{gain} < V_{r3}$$

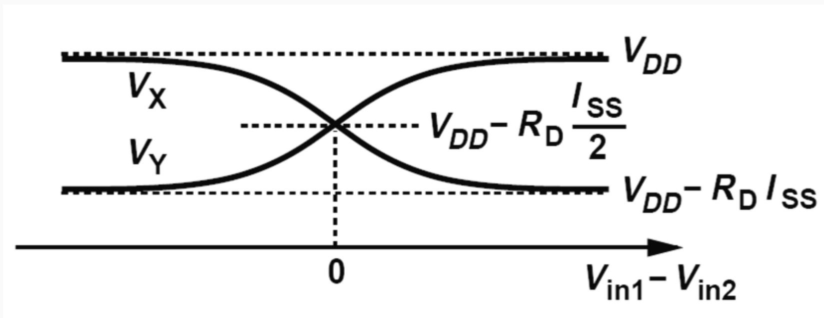
$$\downarrow$$

$$b_3, b_4 = 1, 0$$

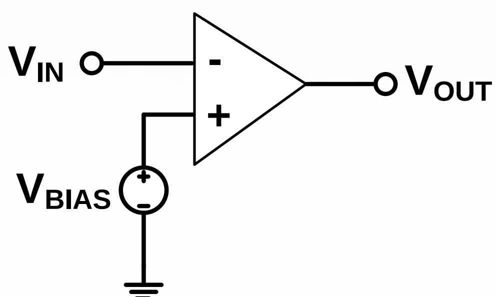
Interpolating A/D converters



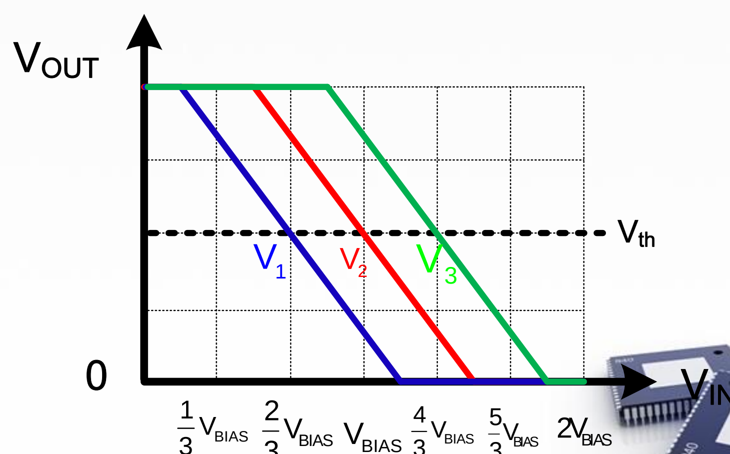
Differential Input amplifier



Variation of output voltage (V_X and V_Y)



- V_1 = 2/3V_{BIAS}, V_2 = V_{BIAS}, V_3 = 4/3V_{BIAS},



Interpolating A/D converters

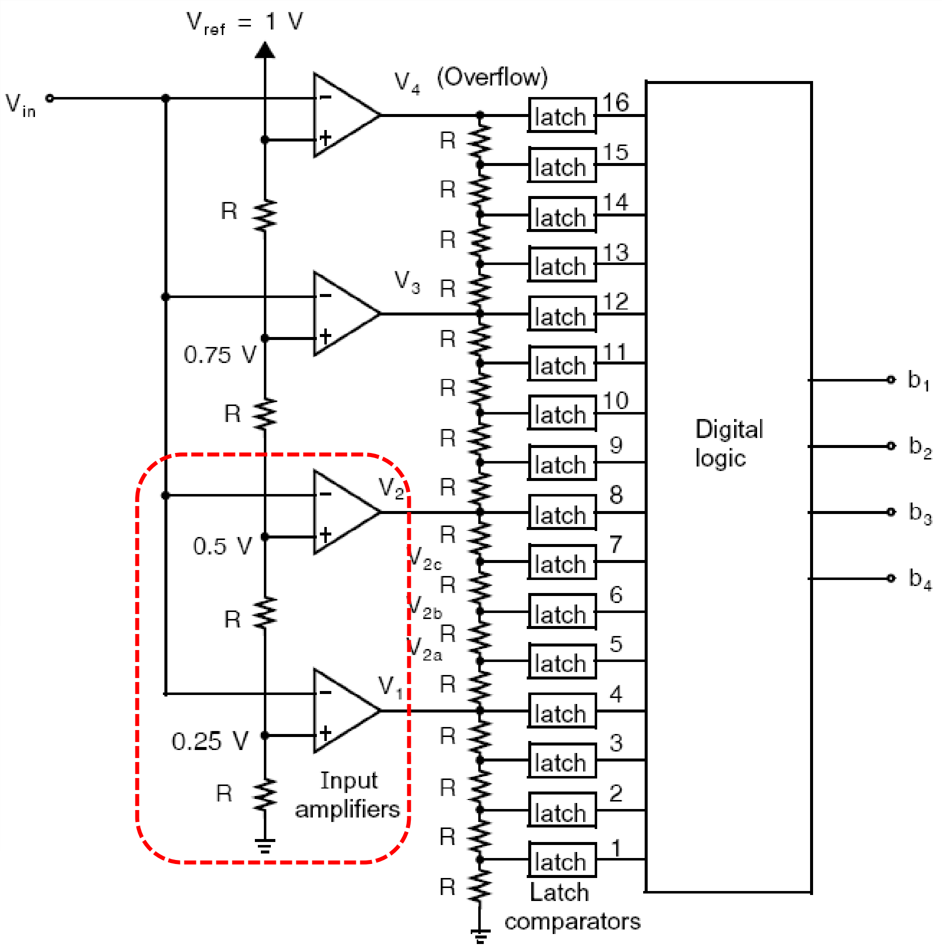


Fig. 17.31 A 4-bit interpolating A/D converter (interpolating factor of 4)

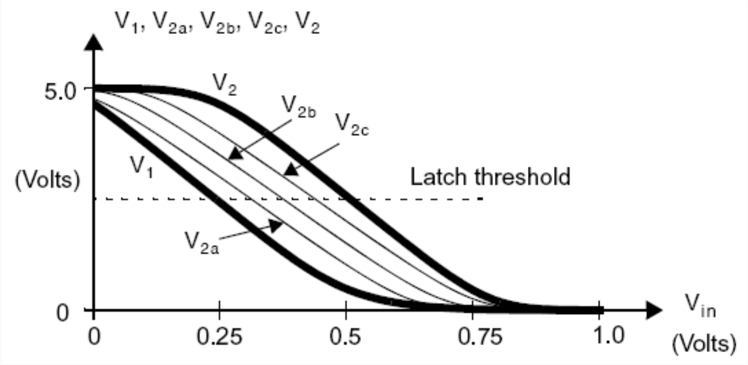


Fig. 17.32 Possible transfer responses for the input-comparator output signals, V1 and V2, and their interpolated signals

monotonic
Input capacitor ↓ (faster than flash)

Latch thresholds is critical
Match delay to latches

Example 4

Find the digital output during the operation of the 3-bit interpolating A/D converter. Assume that V_{in} = 0.23V, 0.6V, V_{ref} = 1V.

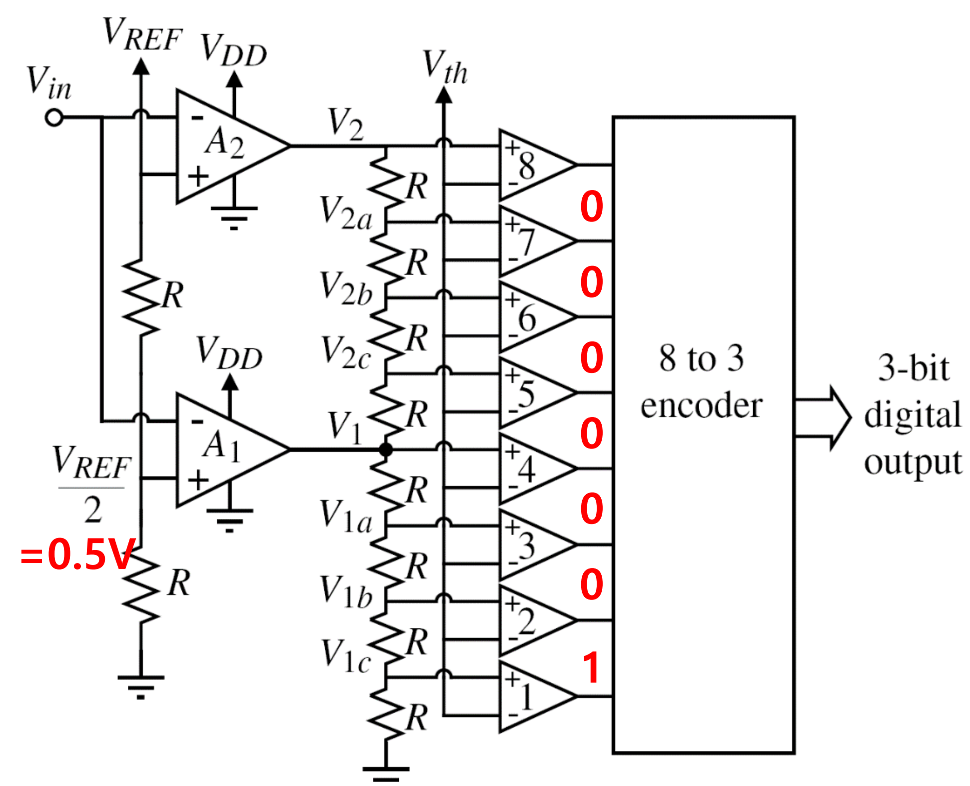
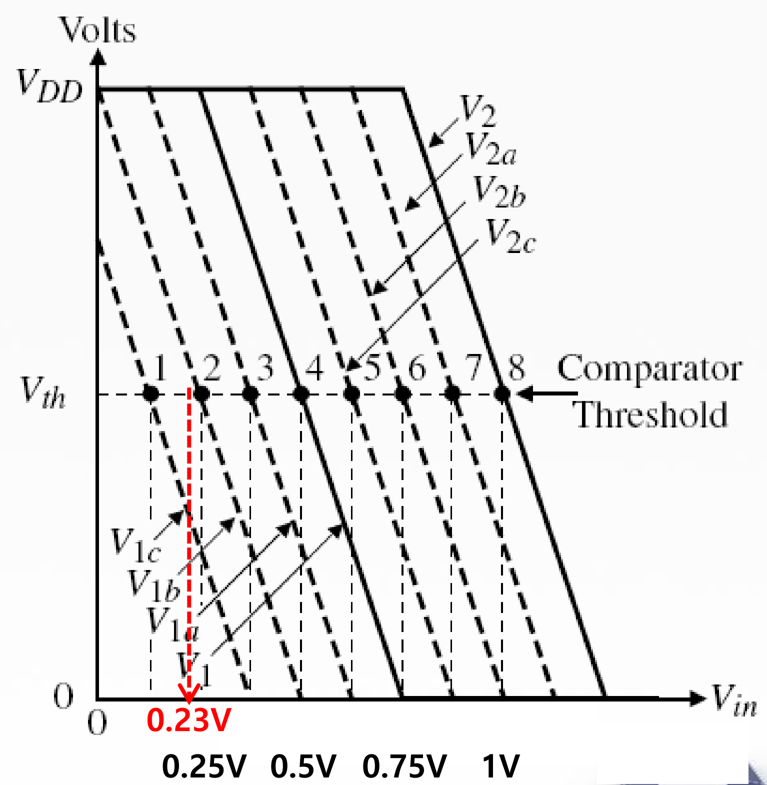


Fig. 17.31 A 3-bit interpolating A/D converter (interpolating factor of 4)

- Vin = 0.23V



Example 5(Cont.)

Find the digital output during the operation of the 3-bit interpolating A/D converter. Assume that V_{in} = 0.23V, 0.6V, V_{ref} = 1V.

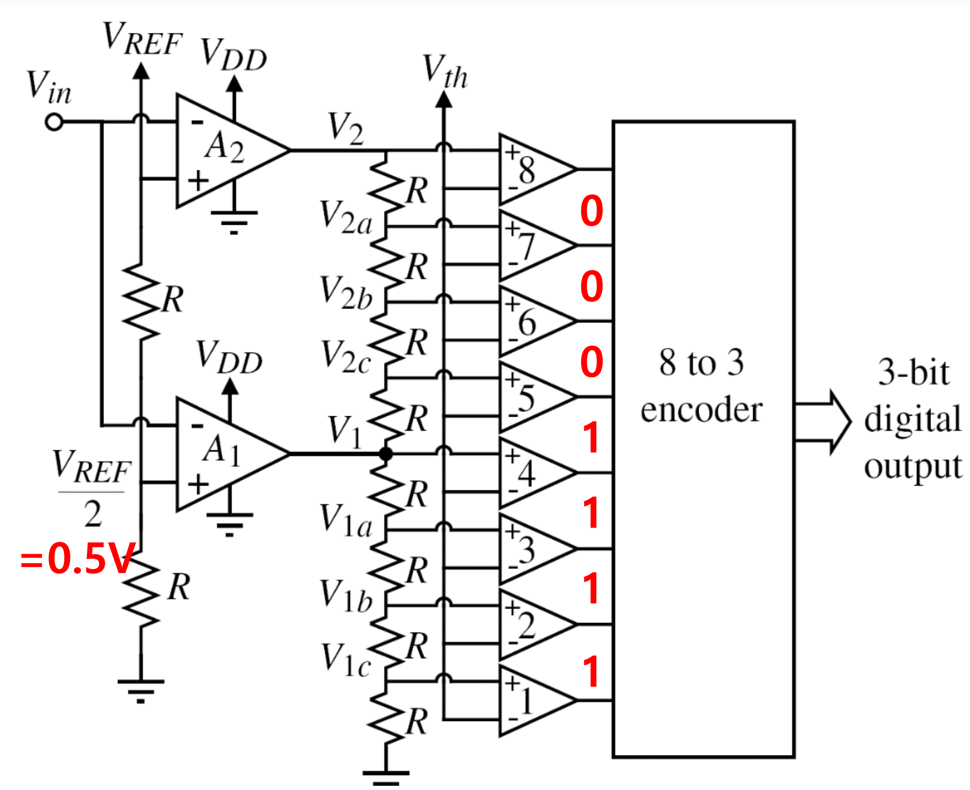


Fig. 17.31 A 3-bit interpolating A/D converter (interpolating factor of 4)

- Vin = 0.6V