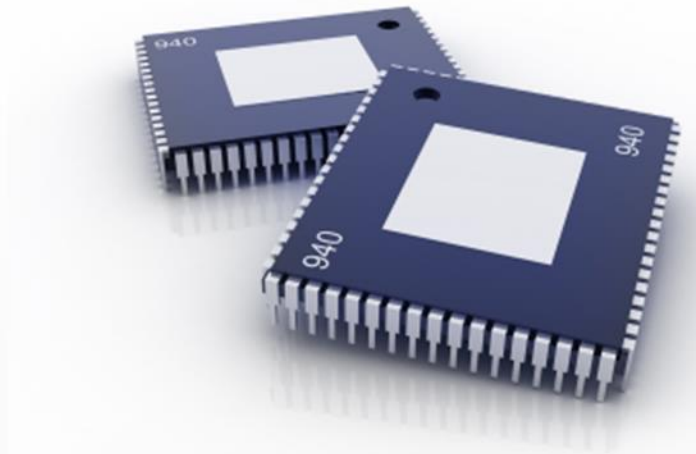

LECTURE 12

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16. Nyquist-Rate D/A Converters

16.1 Decoder-Based Converters

16.2 Binary-Scaled Converters

Resistor-String Converters

The most straightforward approach = **Decoder-based converters**

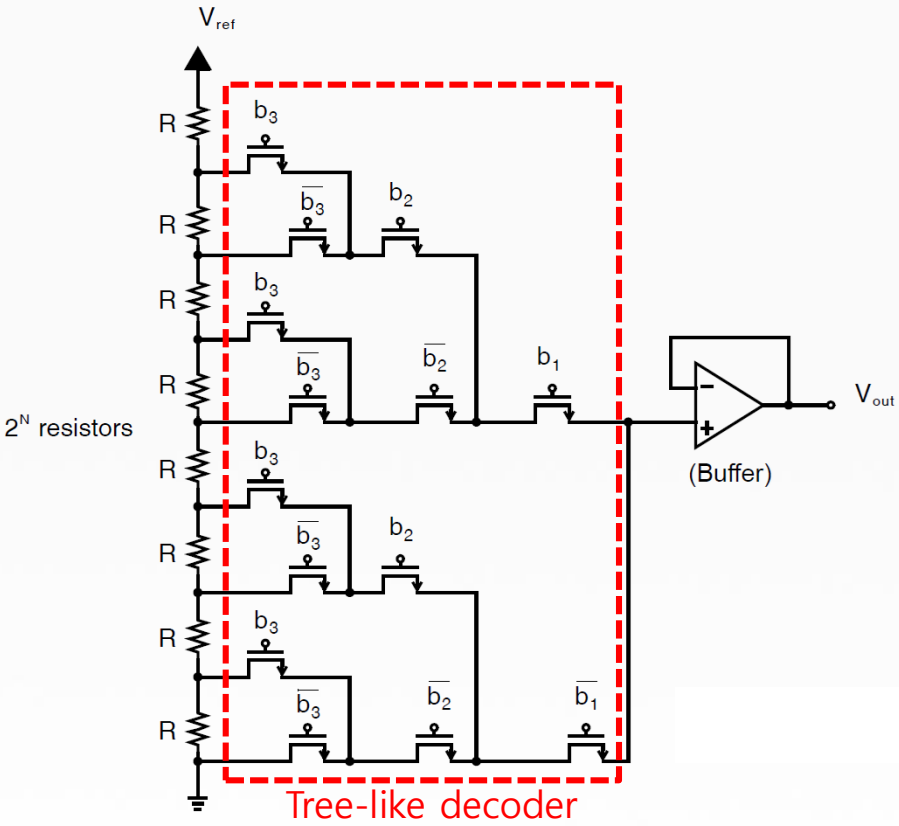


Fig. 16.1 Resistor-string 3-bit D/A converter with a transmission-gate, tree-like decoder

$$V_{out} = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3}$$

스위치의 ON/OFF 동작에
따라 저항에 연결된 전압 중에
오직 하나만이 출력으로 나온다.
이를 아날로그 버퍼에 연결함으로서
원하는 아날로그 전압을 얻는다.

- Monotonic
- Accuracy (depend on R)

- **Limitation on speed**
- Power consumption
- Require 2^N resistors

Example 1

Calculate (a) The **tap voltage** from the resistor string if V_{ref} = 5V
(b) The **output voltage** if the op-amp has an offset voltage of 18mV

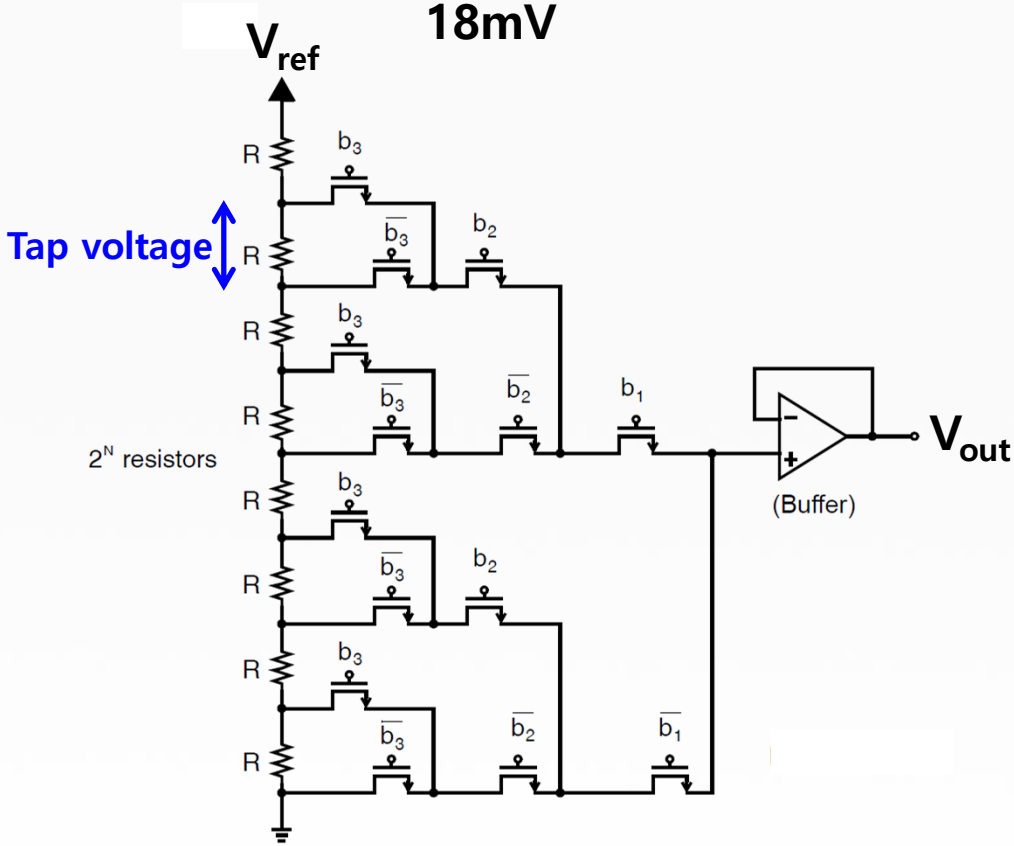
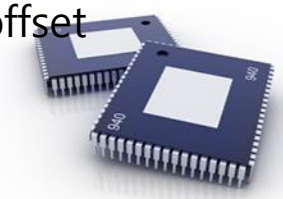


Fig. 16.1 Resistor-string 3-bit D/A converter with a transmission-gate, tree-like decoder

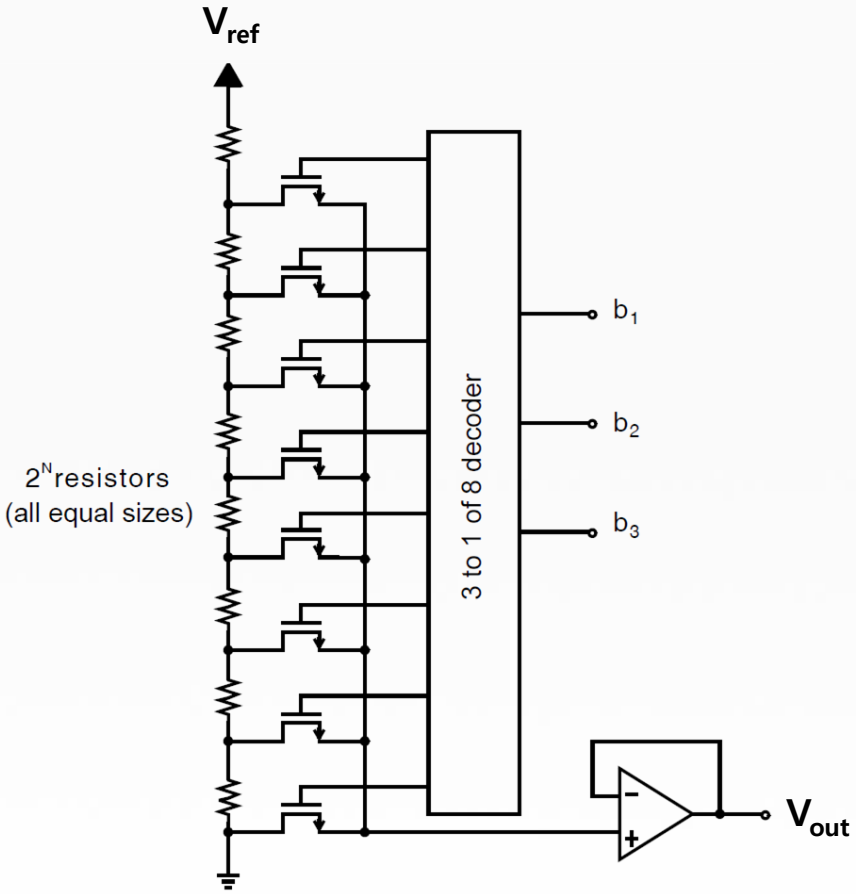
Input Binary Bits			Tap voltage	V_{out}
b3	b2	b1		
0	0	0	0	0.018
0	0	1	0.625 (18mV)	0.643
0	1	0	1.25	1.268
0	1	1	1.875	1.893
1	0	0	2.5	2.518
1	0	1	3.125	3.143
1	1	0	3.75	3.768
1	1	1	4.375	4.393

Need to reduce the offset voltage



Resistor-String Converters

Large series resistors → one resistor



$$V_{out} = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3}$$

스위치가 직렬로 여러 단을 연결되면 동작속도가 기하급수적으로 느려진다. 이를 개선하기 위해 디지털 **Decoder** 를 설계한다.

Switch resistors ↓
Speed ↑

Large capacitive loading
Digital decoder area

Fig. 16.2 Resistor-string 3-bit D/A converter with digital decoding

Folded Resistor-String Converters

To reduce the amount of digital decoding and large capacitive loading

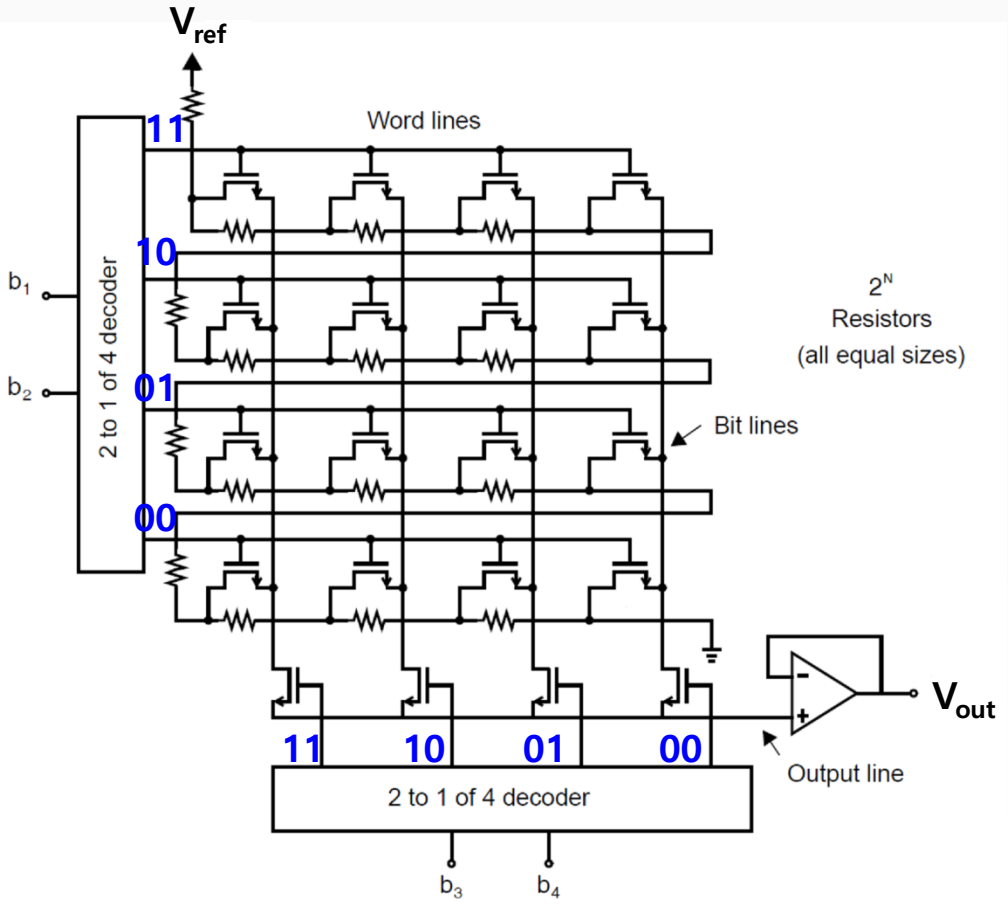


Fig. 16.4 A 4-bit folded resistor-string D/A converter

Similar to digital memory

$$V_{out} = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + b_4 2^{-4}$$

- Reduce the decoding area
- Reduce the capacitive loading

- Power consumption
- **Require 2^N resistors**

Multiple Resistor-String Converters

To reduce the amount of resistors

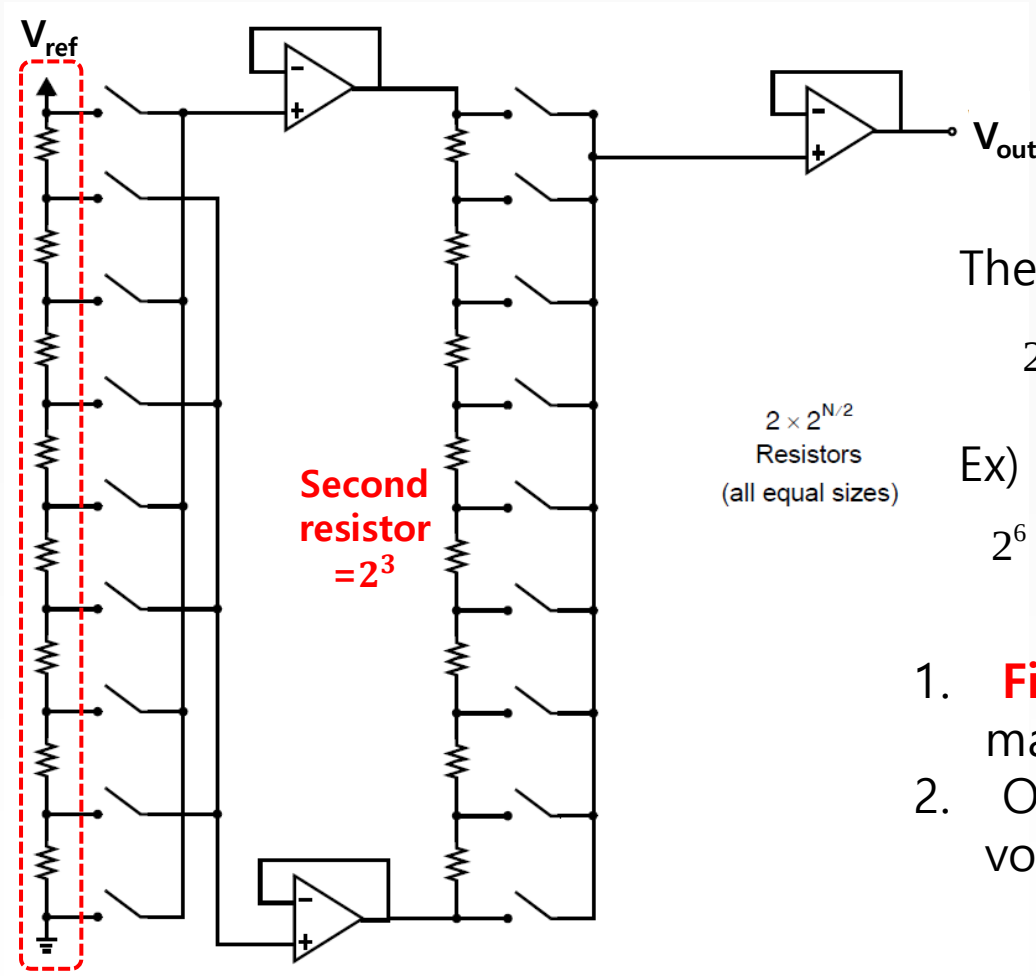


Fig. 16.5 Multiple R-string 6-bit D/A converter

The amount of resistors

$$2^N \Rightarrow 2 \times 2^{N/2}$$

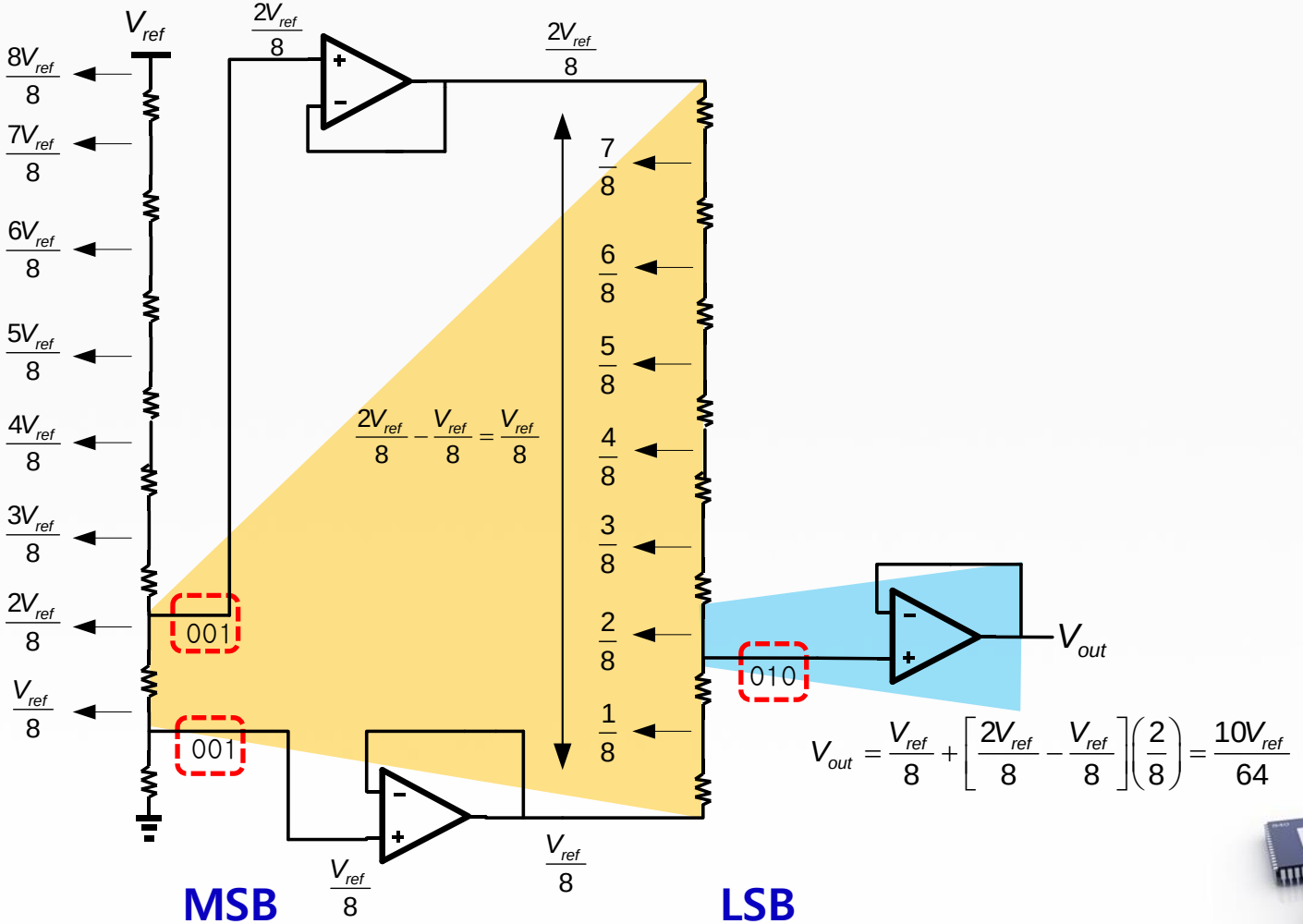
Ex) 6bit

$$2^6 = 64 \Leftrightarrow 2 \times 2^{6/2} = 16$$

1. **First resistor** string should be matched
2. Opamps should have matched, voltage insensitive offset voltage

Multiple Resistor-String Converters

At binary code=001010



Binary-Weighted Resistor Converters

The most popular approach is binary fashion

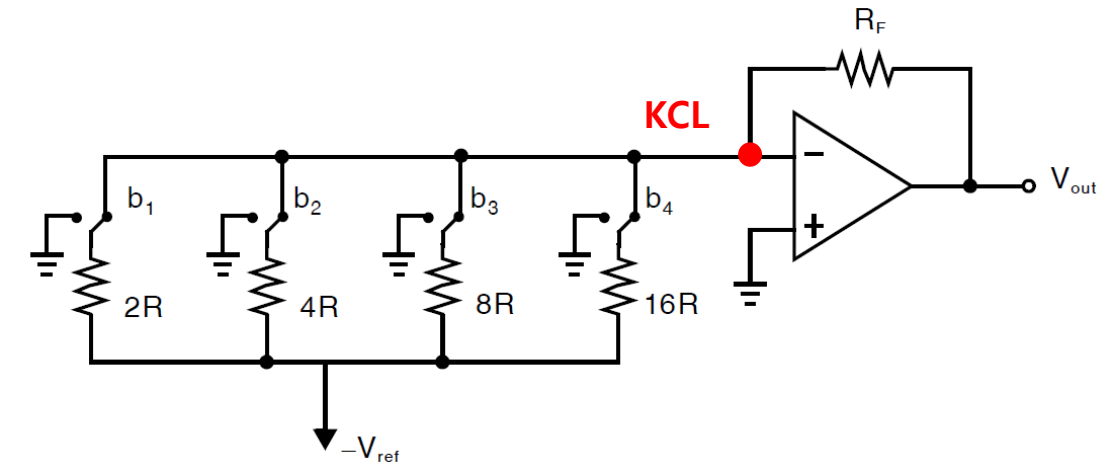


Fig. 16.7 Binary-weighted 4-bit resistor D/A converter

KCL

$$\frac{-V_{ref}}{R_{total}} = \frac{-V_{out}}{R_F}$$

$$V_{out} = -R_F V_{ref}\left(-\frac{b_1}{2R} - \frac{b_2}{4R} - \frac{b_3}{8R} - \cdots\right)$$

$$= \left(\frac{R_F}{R} V_{ref}\right) B_{in} \qquad (16.2)$$

$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots$$

Only N resistors

- No guarantee of monotonicity
- **Resistor and current ratios are on the order of 2^N**

Binary-Weighted Resistor Converters

Reduce the magnitude of resistors

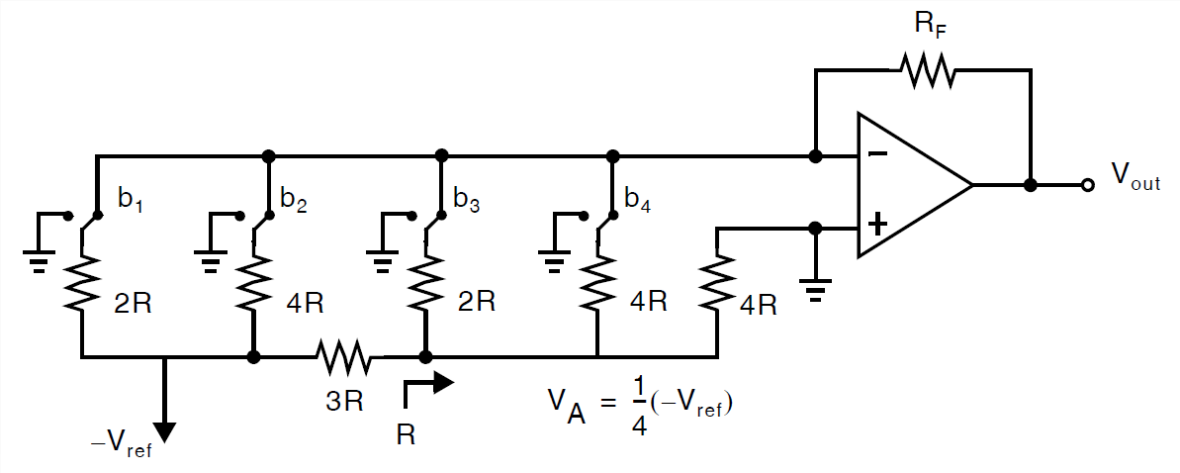


Fig. 16.8 Reduced-resistance-ratio 4-bit D/A converter

$$V_{out} = -R_F V_{ref}\left(-\frac{b_1}{2R} - \frac{b_2}{4R} - \frac{b_3}{8R} - \cdots\right)$$

$$= \left(\frac{R_F}{R} V_{ref}\right) B_{in}$$

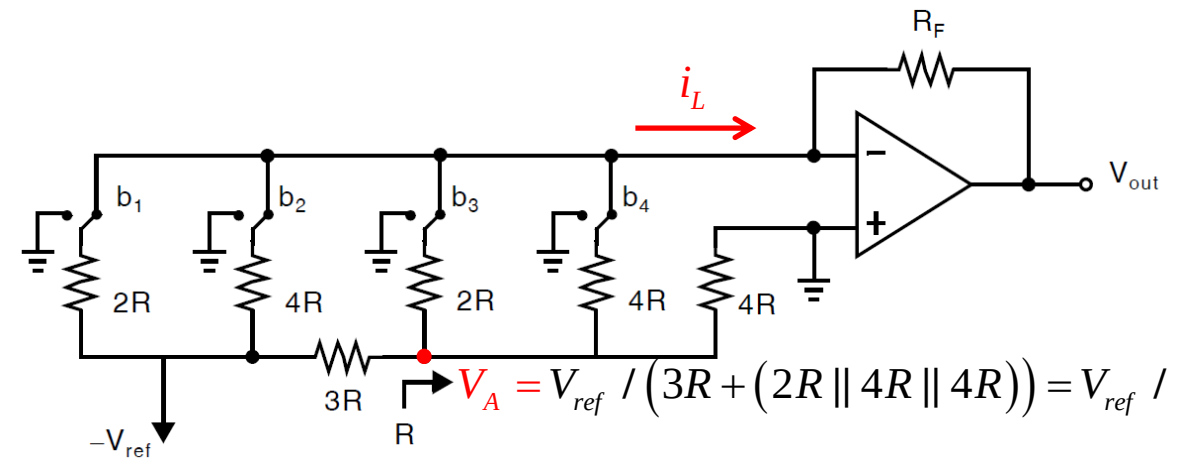
$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots$$

Same relationship as in the previous binary-weighted case

⇨ Arrives at a structure, R-2R ladder

Example 2

Calculate the V_{out} when $b_1b_2b_3b_4 = 0001, 0011, 0101, 1001$



$$V_{out} = \left(\frac{R_F}{R} V_{ref}\right) B_{in} \quad (16.2)$$

Fig. 16.8 Reduced-resistance-ratio 4-bit D/A converter

- $b_1b_2b_3b_4 = 0001$

$$i_L = V_{ref} / 16R$$

$$V_{out} = \frac{R_F}{16R} V_{ref}$$

- $b_1b_2b_3b_4 = 0011$

$$i_L = 3V_{ref} / 16R$$

$$V_{out} = \frac{3R_F}{16R} V_{ref}$$

- $b_1b_2b_3b_4 = 0101$

$$i_L = V_{ref} / 4R + V_{ref} / 16R$$

$$V_{out} = \frac{5R_F}{16R} V_{ref}$$

- $b_1b_2b_3b_4 = 1001$

$$i_L = V_{ref} / 2R + V_{ref} / 16R$$

$$V_{out} = \frac{9R_F}{16R} V_{ref}$$

R-2R Based D/A Converters

A very popular architecture for D/A converter

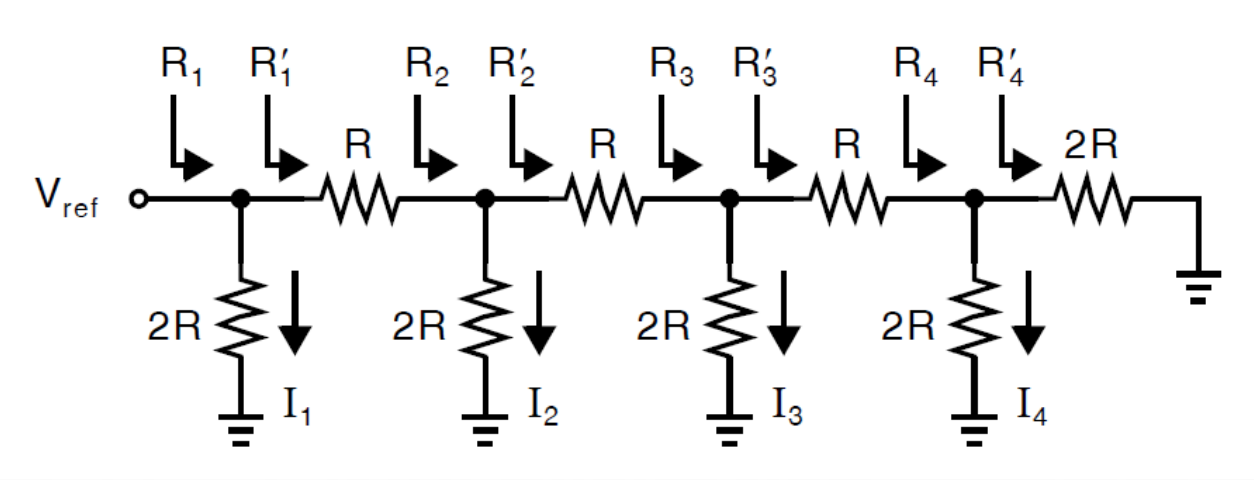


Fig. 16.9 R-2R-Based Converters

$$R_4' = 2R$$
$$R_4 = 2R \,||\, 2R = R$$
$$R_3' = R + R_4 = 2R \quad (16.4)$$
$$R_3 = 2R \,||\, R_3' = R$$

$$I_1 = \frac{V_{ref}}{2R} \quad (16.5)$$

$$I_2 = \frac{V_{ref}}{4R} \quad (16.6)$$

$$I_3 = \frac{V_{ref}}{8R} \quad (16.7)$$

R-2R Based D/A Converters

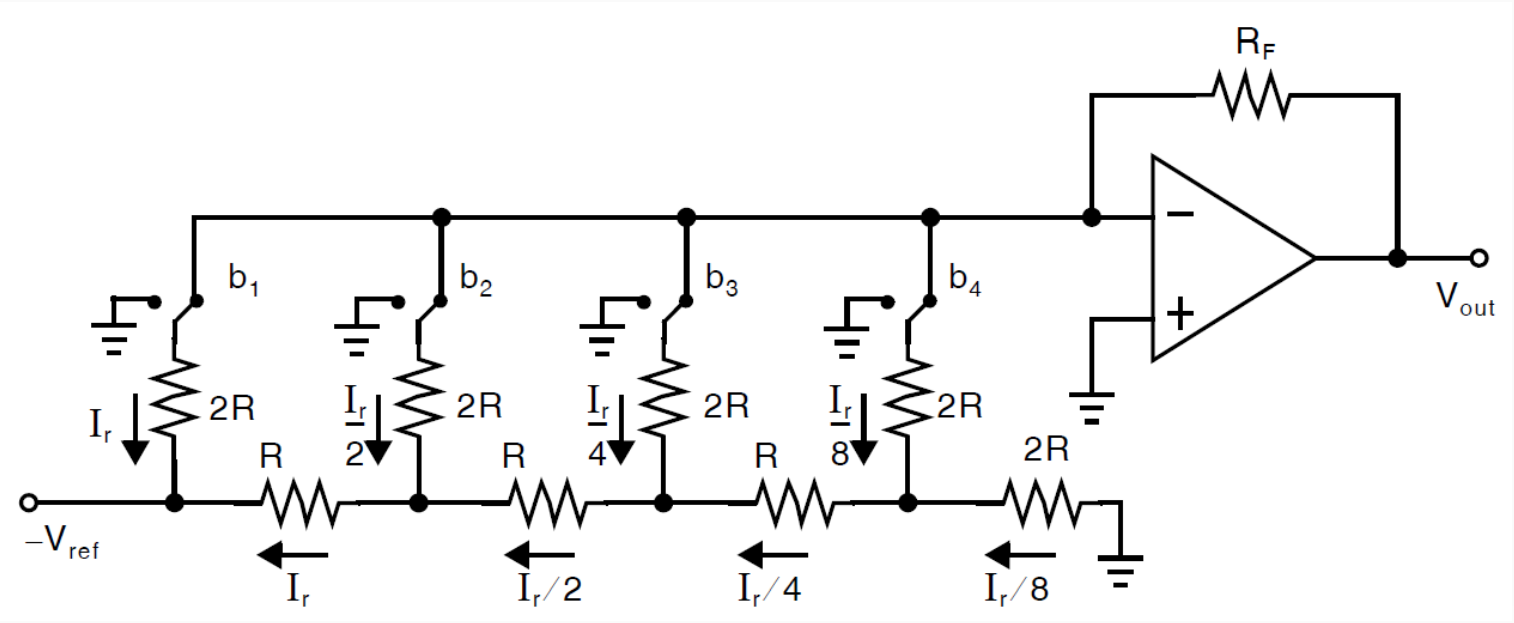


Fig. 16.10 4-bit R-2R-Based Converters

$$I_r = \frac{V_{ref}}{2R} \qquad (16.8)$$

$$V_{out} = R_F \sum_{i=1}^{N} \frac{b_i I_r}{2^{i-1}} = V_{ref} \left(\frac{R_F}{R} \right) \sum_{i=1}^{N} \frac{b_i}{2^i} \qquad (16.9)$$

- Small size
- Good matching (only R and 2R)

- Should scale switch sizes for good accuracy(unequal current)
- **Offset**

Example 3

Calculate the V_{out} when $b_1b_2b_3b_4$ = 0010, 1001, 0111

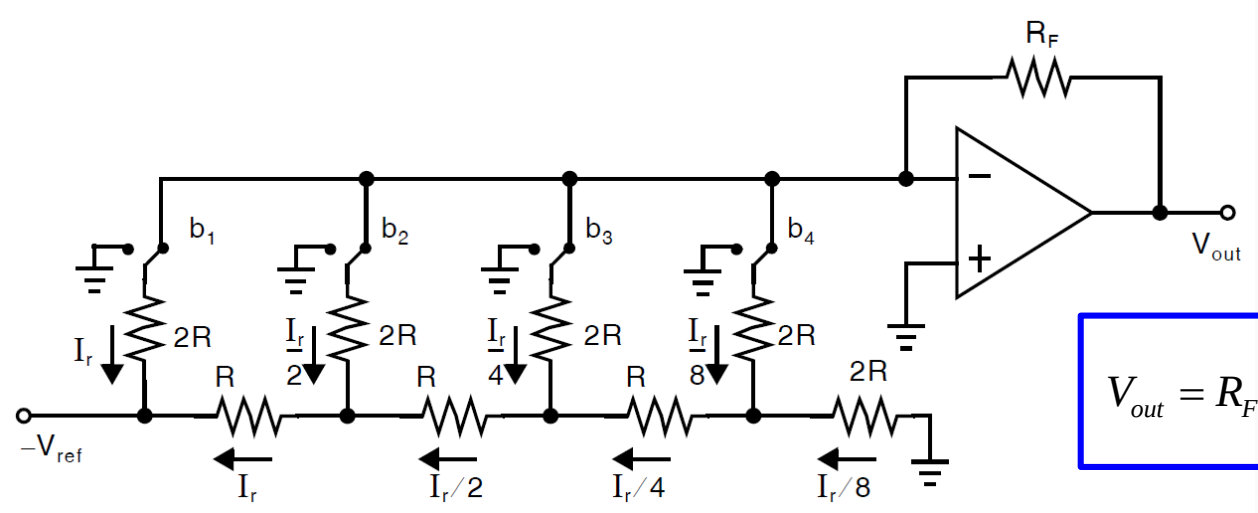


Fig. 16.10 4-bit R-2R-Based Converters

$$V_{out} = R_F \sum_{i=1}^{N} \frac{b_i I_r}{2^{i-1}} = V_{ref}\left(\frac{R_F}{R}\right)\sum_{i=1}^{N}\frac{b_i}{2^i} \quad (16.9)$$

- $b_1b_2b_3b_4$ = 0010

$$V_{out} = V_{ref}\left(\frac{R_F}{R}\right)\cdot\left(\frac{1}{8}\right)$$
$$= V_{ref}\left(\frac{R_F}{8R}\right)$$

- $b_1b_2b_3b_4$ = 1001

$$V_{out} = V_{ref}\left(\frac{R_F}{R}\right)\cdot\left(\frac{1}{2}+\frac{1}{16}\right)$$
$$= V_{ref}\left(\frac{9R_F}{16R}\right)$$

- $b_1b_2b_3b_4$ = 0111

$$V_{out} = V_{ref}\left(\frac{R_F}{R}\right)\cdot\left(\frac{1}{4}+\frac{1}{8}+\frac{1}{16}\right)$$
$$= V_{ref}\left(\frac{7R_F}{16R}\right)$$

Charge-Redistribution Switched-Capacitor Converters

Replace resistors to capacitor array

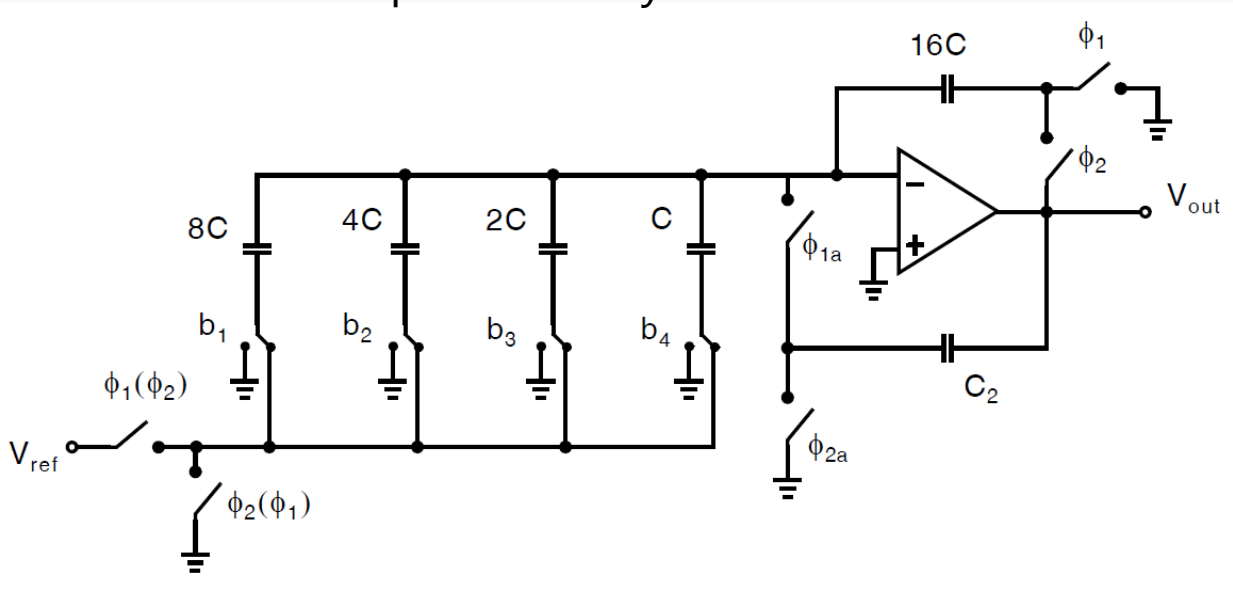


Fig. 16.12 Binary-array charge-redistribution D/A converter

Resistors ⇨ **Capacitors**

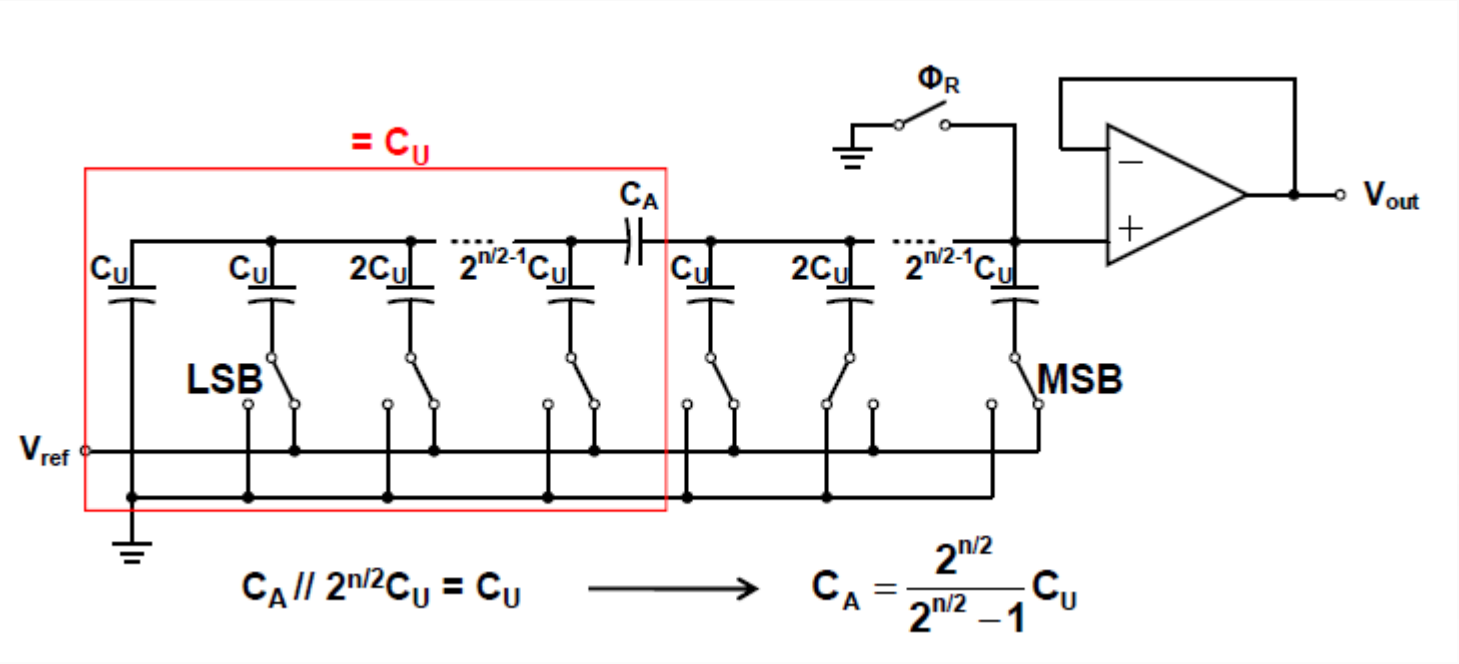
1. Insensitive to opamp input offset
2. Doesn't affect opamp gain

$$V_{out} = \left(\frac{C}{16C} V_{ref} \right) B_{in}$$

$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots$$

Charge-Redistribution Switched-Capacitor Converters

To reduce the capacitor



- 12-bit full binary: $C_{TOT} = 2_{12}C_U$.
- With attenuation capacitor.
  - $C_A = 1.015873C_U$.
  - $C_{TOT} = 2 \times 2_6C_U + 1.015873C_U$.
  - Matching is difficult.
  - Even division (n/2) is not necessary. m-bit (MSBs) & n-bit (LSBs) division possible.